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(54) Package to board variable pitch tab.

(57) A variable pitch tab leadframe assembly (103) has a plurality of patterned conductive elements (107) for transmitting input and output signals to bonding locations on an electronic device. The leadframe assembly comprises conductive elements with a variable pitch to accommodate a plurality of standard pitch bond site printed circuit board footprints.

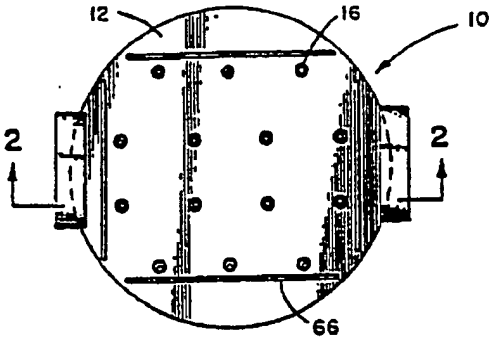

FIG. 1

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PACKAGE TO BOARD VARIABLE PITCH TAB

Field of the Invention

The present invention relates to the field of electronic component manufacturing and packaging.

Background of the Invention

A problem in the prior art of electronic component packaging includes inefficient steps in the production of leadframes for bonding with variably sized and pitched component packages. The substantial inefficiencies inherent in requiring different leadframes to be manufactured for connecting different packages to printed circuit boards is both costly and wasteful. However, by providing a universal tab leadframe which may be utilized, by only slight modification, with variably pitched packages, then cost and material savings combine to greatly improve the manufacturing and packaging processes. The present package to board variable pitch tab leadframe invention overcomes the problems identified above.

Summary of the Invention

The present invention is a variable pitch tab leadframe assembly. The leadframe assembly comprises a plurality of patterned conductive elements for transmitting input and output signals to bonding locations on an electronic device. The leadframe assembly comprises conductive elements with a variable pitch to accommodate a plurality of standard pitch bond site printed circuit board footprints.

Brief Description of the Drawings

Figure 1 is a top plan view of a shadow mask and die assembly showing shadow mask vias.

Figure 2 is a side elevation cross section view taken generally along line 2-2 of Figure 1 showing a shadow mask removably attach d to a di representing a waf r or chip.

Figure 3 is an enlarged cross sectional elevation view of a portion of the die shown in Figure 2 illustrating deposited solderable material on a portion of the die after the mask is removed from the die.

Figures 4a and 4b are cross section elevation views of a prior art leadframe/gold bump bonding process showing both incomplete leadframe-to-gold bump bonding and a fractured die.

Figures 5a and 5b are cross section elevation views of a leadframe with organic standoff means arranged for bonding with solder bumps.

Figure 6 is a side elevation view depicting a schematic prior art tin coated copper leadframe being positioned for bonding to a gold metalization bump.

Figure 7 is a side elevation view depicting a schematic copper leadframe shown in position for bonding to a tin cap solid base metalization bump.

Figure 8 is a cross section elevation view of a prior art gold bump manufactured by a spin-on resist process.

Figure 9 is a cross section elevation view of a spun-on resist solid base bump with a tin cap.

Figure 10 is a cross section elevation view of a prior art vertical wall gold bump manufactured by a dry film resist process.

Figure 11 is a cross section elevation view of a vertical wall dry film resist solid base bump with a tin cap.

Figure 12 is a top fragmentary view of a variable pitch tab leadframe.

Figure 13 is a top plan view of a representative tape leadframe illustrating four sections generally analogous to that shown in Figure 6 to form a complete variable pitch tab leadframe about a central package area.

Figure 14 is a top plan schematic view of the second end portions of adjacent conductive elements of a variable pitch tab leadframe having a first pitch at bond pads of a next level of packaging.

Figure 15 is a top plan schematic view of the second end portions of adjacent conductive elements of a variable pitch tab leadframe having a second pitch at bond pads of a next level of packaging.

Figure 16 is a top plan schematic view of the second end portions of adjacent conductive elements of a variable pitch tab leadframe having a third pitch at bond pads of a next level of packaging.

Detailed Description of the Preferred Embodiments

Detailed preferred embodiments of the present invention are disclosed. It is to be understood,

however, that the disclosed embodiments are merely exemplary of the invention, which may be embodied in various forms. Therefore, specific structural and functional details disclosed are not to be interpreted as limiting, but rather as a representative basis for teaching one skilled in the art to variously employ the present invention in virtually any appropriately detailed system or structure. It will be understood that in some circumstances relevant material thicknesses and relative component sizes may be shown exaggerated to facilitate an understanding of the invention.

Inventions described in the present application relate to improvements in manufacturing, bonding, and packaging of electronic components to achieve improved reliability, improved yield, and greater material and manufacturing efficiencies. The improvements comprise unique features including etched shadow mask construction, conductive metalized bump composition, and preferred structure of tape leadframes.

Referring to Figure 1, an exemplary mask 10 is illustrated. It is appreciated that masks, also known as shadow masks or vapor deposition masks, are variously constructed and shaped; however, the basic function of masks is to provide vapor deposition patterns for conductive material to be evaporated onto a die thereunder. Accordingly, mask 10 comprises a mask top surface 12 which defines apertures or vias 16. Mask 10 is removably mounted on a surface of a die and positioned in a chamber in which evaporation and deposition of solderable material will occur. During the evaporation and deposition process, the solderable material passes through vias 16 in mask 10 and is deposited in a pattern on the die. This provides a pattern of solderable material on the die for later reflowing, bonding, or other operations.

Frequently, prior art masks experience warping or other reshaping so that vaporized solderable material passes through the vias and is deposited on various portions of the die which were not directly beneath each via area. This results in unwanted electrical shorts being created on the die. Yet another problem exists with prior art masks wherein a substantial portion of the mask surface is in contact with the die when the mask is agitated or slightly moved. This often results in scratching of the die surfaces. These problems substantially reduce the yield of reliable die during the production process. Due to the expensive recovery required in repair of poorly manufactured or damaged dies, many such devices are discarded. It is appreciated, therefore, that the associated yield problem results in waste and inefficiency in the industry.

Figure 2 is a side elevation cross section view taken generally along lines 2-2 of Figure 1 showing mask 10 removably mounted onto die 24 by mounting means 20. Die 24 may comprise a semiconductor chip, or a wafer comprising numerous semiconductor chips. Die 24 may comprise various materials and layers, however, a representative material combination in the die upper passivation region 25 includes a passivation portion 25a, such as silicon nitride, or more generally an insulator material, and a metalized portion 25b, such as aluminum, or more generally a conductive metalization. As is well known in the field, metalized portions 25b comprise conductive interconnects and are, therefore, deposition sites for later depositing of the vaporized solderable material. More specifically, interface metalization 28, shown in Figure 3, is commonly deposited first onto metalized portion 25b, and then solderable bump material 30, also shown in Figure 3, is then vapor deposited through vias 16 onto interface metalization 28.

Figure 2 shows die 24 comprising top surface 34 and bottom surface 36. Figures 2 and 3 therefore illustrate die 24 having a plurality of deposit sites etched or otherwise positioned to provide solderable material in the form of bumps onto interface metalization 28, and extending generally from die top surface 34. In order to precisely position vaporized solderable material at these particular desired deposition sites, a mask of suitable rigidity and via pattern must be used. Such masks are frequently made of metallic materials, as preferably is mask 10, which is typically constructed of molybdenum; however, other materials may be utilized such as glass or plastic.

Mask 10 comprises mask top surface 12 which functions as an outer surface facing away from die 24 in operation, and which is located opposite mask bottom surface 13. As shown in Figure 2, vias 16 extend through mask 10 between top surface 12 and bottom surface 13 to permit vaporized bonding metals to pass through the mask and to deposit onto predetermined locations of die 24. As further shown in Figure 2, mask bottom surface 13 comprises a plurality of recessed regions 44. Regions 44 are constructed to minimize the area of mask 10 in contact with die 24 during the vapor deposition process. Moreover, the arrangement of recessed regions 44 in relation to bottom surface 13 surrounding vias 16 provides for substantially full mask thickness via regions having a width labelled R which provide damming action about the via to retain the vapor deposit within the predetermined deposit sites of die 24 defined by the via regions.

Another way of describing the relation between recessed regions 44 and vias 16 is to describe the recessed regions 44 as having a base surface 47 which are constructed and arranged for placement at a distanc D from die surface 34. Thus, mask 10 bottom surface 13 includes etched recessed re-

gions 44 which define a projection 49 located around each via 16. Projections 49 extend from the plane or planes 50 which includes base surfaces 47 of etched recessed regions 44 to minimize the contact area of mask 10, to only that area of bottom surface 13, in contact with die 24 during the entire process of vapor deposition.

By reducing the surface area of mask 10 actually in contact with die 24, the risk of the mask damaging the die is greatly reduced. Moreover, this mask construction allows the clamping or retaining force of mounting means 20 to be advantageously focused onto the areas defined by bottom surface 13 immediately surrounding vias 16. Thus, a secure fit of mask 10 results and unwanted deposition of solderable material beyond the area on the die defined by the diameters of each via 16, shown in Figure 2 as R', is prevented. Prior art shadow masks have failed to adequately contain solderable materials and have frequently resulted in undesired and uncontrolled seepage of such materials between predetermined deposition sites, resulting in electrical shorts and reduced capabilities of the devices involved.

It is to be understood that as the number of vias on mask 10 increases, an increasing area of mask bottom surface 13 is required to achieve the objectives stated above. Also, as the density of vias 16 increases, then undesired flexing or loss of rigidity of mask 10 may occur. Therefore, reinforcing ridges 66, shown in Figures 1 and 2, may be utilized for stiffening mask 10. Reinforcing ridges 66 may be arranged in various orientations and shapes to achieve the advantages within the scope of this invention. Indeed, reinforcing ridges 66 need not be limited to protrusions from top surface 12 but instead may comprise material which is hardened in relation to the mask material comprising the remainder of mask 10.

In a preferred embodiment, mask 10 comprises a molybdenum mask having a full thickness of 4 mils. Preferred mask 10 may be used with a die having passivation and metalization combined thickness of approximately 20 mils. Moreover, such a combination would provide means for depositing about a .5 micron thin film interface metalization 28, and a subsequent 100 micron thickness solderable material 30, as shown generally and not to scale in Figure 3. It is appreciated that sizes and shapes shown herein may vary considerably with each production requirement. The substantial reduction of contact surface area between mask 10 and die 24 is most relevant, as is the manner in which mask 10 prevents unwanted deposition of conductiv metalization onto areas of die 24 beyond th via areas labelled by diameter R'.

A method of manufacturing a damage reducing tched shadow mask 10 for providing vapor deposition patterns of bonding metals onto a surface of die 24 is also provided. This method preferably comprises the steps of providing a nonwettable shadow mask 10 having top surface 12 and bottom surface 13; creating vias 16 extending through mask 10; and etching portions of mask 10 bottom surface 13 to provide recessed regions 44 and substantially full thickness regions (having height labelled E and width comprising the thickness of R-R' as shown in Figure 2), the recessed regions 44 providing for a reduced surface area in contact with die 24 during a vapor deposition process. The etching step may further comprise providing projections 49 or ridges extending annularly from vias 16 at bottom surface 13 of mask 10. Mask 10 permits manufacture and deposition through evaporation of a plurality of bumps comprising solderable conductive bump material 30, Figure 3, and which is shown in shadow 31 in a reflowed configuration.

Within the field of electronic component manufacturing and packaging, serious problems exist due to inadequate uniformity of conductive bump height, unacceptable organic matter within packages, fatigue-prone bonds, and temperature sensitive components. An example of non-uniform conductive bump heights is shown in Figure 4a in which prior art gold bumps 61a, 61b, 61c, and 61d are arranged on die 62. As illustrated, bumps 61a, 61b, 61c, and 61d have different heights representative of the non-uniformity of bump heights often present in such structures. In a typical prior art process, a representative leadframe assembly is positioned over die 62 and the bumps, with the leadframe assembly comprising conductive metal leads 63.

Figure 4b illustrates the structures of Figure 4a after a planar bonding force has been applied to leads 63 by bonding tip means 66. As is shown in the figure, the bonding force has caused die 62 to fracture below gold bump 61b due to the high bump height of that bump. As is also shown, leads 63 have contacted and bonded with correspondingly located bumps 61b and 61d. However, gold bump 61c has not bonded with its lead due to the short bump height of bump 61c. This results in non-conductivity and improper performance of a device using die 62 and relying on a bond between bump 61c and its lead.

Figure 5a and 5b are cross section elevation views of a leadframe with organic standoff means arranged for bonding with solder bumps. Height standoff means 64 is commonly provided t prevent overcompression of l ads 63 into the conductive bonding material of relatively soft bumps such as solder bumps 61e which do not maintain a uniform standoff height when bonding tip means 66 is brought into contact with leads 63 to form a

connection between leads 63 and die 62 via the solder bump 61e. Height standoff means 64, or dielectric means, is frequently constructed of organic material which is subject to moisture collection and long term deterioration.

The present tin cap on solid base bump invention solves the problems illustrated in Figures 4b and 5b. With the present tin cap on solid base bump invention, cracking of die 62 under prior art gold bumps such as 61b is substantially reduced when such prior art gold bumps are replaced by the present tin cap on solid base bump invention. Further, open connections such as shown above prior art gold bump 61c in Figure 4b are substantially reduced when such prior art gold bumps are replaced by the present tin cap on solid base bump invention. In addition, when the present tin cap on solid base bump invention is used to replace prior art solder bumps 61e, height standoff means 64 comprising organic material can be eliminated, thus creating the option of a package free of organic material, consistent with requirements such as those of U.S. Department of Defense Military Standard 38510.

It is to be understood that within the field of electronic component manufacturing and bonding another problem exists with respect to inadequate means for strong and efficient bonding of leads to various devices. For example, the bonding forces and temperatures needed for bonding prior art leads often caused cracking of integrated circuit devices and open bonds. These phenomena led to plating of leads, commonly copper leads, with tin in order to lower the force and temperature requirements for bonding. However, that solution led to yet another problem known as whiskering, which occurred principally during the tin plating process. This problem relates particularly to copper leads 76 such as depicted in Figure 6 that are plated or coated with a solderable material 78 such as tin. Plated lead 76 is shown prior to bonding to a conductive metalized bump 80 located on a semiconductor device 82. This new problem was addressed in the art either by providing additional processes to achieve tin stress relief or by plating the copper or other metal leadframes with gold or other metals. Those solutions, however, are relatively very time consuming and expensive, and are therefore less preferable to the low cost solution of the present tin cap on solid base, such as gold, bump invention.

As illustrated in Figure 7, conductive lead 84, such as a portion of a conductive metalized leadframe, is provided. A schematic conductive metalized bump 98 is also shown positioned on a die 90. Bump 98 preferably comprises a bump lower portion 92 comprising a gold base material of substantially 100% by weight gold to provide a substantially fixed standoff height during the bonding process. Bump 98 preferably also comprises a bump upper portion 94 comprising an effective amount of tin deposited on a top surface 97 of the gold base material comprising the bump lower portion 92. Preferred tin cap on gold base bump 98 provides improved means for interconnecting electronic components and comprises improved fatigue and expansion coefficient properties over solder bumps on dies. This gold-tin combination bond provides a high strength reflowable alloy.

As an alternative to lower portion 92 comprising substantially 100% by weight of gold, a suitable base material may be comprised of at least one metal selected from a group consisting of chrome, nickel, titanium-tungsten, cobalt, and copper. Of particular relevance, however, is the manner in which the bump lower portion 92 provides effective standoff height during the bonding process and the manner in which the tin cap marerial permits lead travel well into the bump structures during the bonding process so that the bump height uniformity tolerances may be less severe. It is to be understood, however, that a tin cap on a solid base bump may be employed without using only a gold base. For example, as indicated above, a solid base of nickel or other suitable conductive material is within the scope of this invention.

Further, by use of preferred bump 98, the previously identified problems of the prior art are solved using a relatively inexpensive combination and arrangement of materials. By plating tin on top of a gold base and then reflowing the tin during a bonding process, a gold-tin joint is achieved between a die and a leadframe. This provides for the manufacture of gold tin alloy bumps which simplify the leadframe-to-chip bonding process as compared with tin or gold plated copper leads and gold bumps, which often result in a cracked die, or which display the tin whiskering described above.

The use of a bump comprising a tin cap upper portion 94 on a solid base lower portion 92, provides standoff height independent of any requirement for organic material attached to either the lead 84 or the die 90. Accordingly, a bump is provided for use in interconnecting electronic components which meets the organic matter prohibition of U.S. Department of Defense Military Standard 38510, and similarly restricted military standards. This results in substantially improved reliability for electronic components. Moreover, such construction facilitates the type of mass bonding known as "gang bonding" for high-density electronic devices by easing the restrictions for planarity with respect to bond height. In other words, the individual bond heights of a plurality of bumps 98 need not be precisely the same due to the phenomenon of the tin material comprising the bump upper portion 94

providing relief for proper penetration of lead 84. This structure also facilitates repair or rework of bumps to provide overall manufacturing cost savings.

Prior art bumps comprising only gold, such as bumps 99, 100 in Figures 8 and 10, must have a height uniformity of within ± 1 micrometer. However, a preferred tin cap on solid base bump, such as bumps 101, 102 in Figures 9 and 11, allow about ± 5 micrometers of bump height non-uniformity. Thus, preferred tin cap on solid base, such as a gold or nickel base, bumps 88, 101, and 102 provide non-organic non-collapsible height standoff means while also permitting sufficient travel or penetration of conductive leads into the tin caps to achieve higher reliability during bonding over prior art bump structures.

Figures 8 and 9 show bumps manufactured using spin-on resist processes while Figures 10 and 11 show bumps manufactured using dry film resist processes. Note the novel structures shown in the tin capped bumps 101, 102 of Figures 9 and 11 respectively. These tin cap on solid base bumps overcome the bond reliability and organic matter problems of the prior art. This novel bump structure also overcomes the prior art bond site fatigue and tin whiskering problems. Even further, the high strength tin cap on solid base bump invention permits use of materials having compatible coefficients of expansion and which permit reflow and bonding at temperatures and pressures which are lower than in the prior art.

In operation, a preferred tin cap on solid base bump 98 typically comprises approximately 5 microns of tin positioned on top surface 97 of bump lower portion 92, shown generally in Figure 7, in which the bump lower portion 92 material typically comprises approximately 30 microns of solid base material, such as gold or the like. Preferably, the bonding process uses a furnace bond process to further minimize the shock of bonding leads 84 onto die 90. Thus, a method of providing a low temperature and high reliability bond between electronic components is provided. This method includes the steps of providing first and second electronic components; providing a bump for placement onto the first electronic component, the bump having a lower portion 92 comprising an effective amount of solid or non-collapsible conductive metal (e.g. gold or nickel) base material to provide non-organic standoff height during the bonding process; placing an effective amount of tin bonding material n top of the solid bas material; positioning the second electronic component proximate the tin, as shown in Figures 6 and 7 by force labels F and F′ respectively; and reflowing the tin to provide a bond between the first and second electronic components and to provid a bond between the solid base material and the tin bonding material. This method preferably includes a first electronic component comprising a lead, such as lead 84, of a leadframe, and a second electronic component comprising a die, such as die 90, which may be a semiconductor chip or wafer, or similar bump-carrying device. A preferred method of providing a low-temperature high-reliability bond between electronic components preferably comprises the step of reflowing the tin within a furnace heater.

Another method is provided according to the present tin cap on solid base bump invention. This method includes providing furnace bonding of a semiconductor chip to the conductive elements of a leadframe. This method comprises the steps of positioning a semiconductor chip comprising a plurality of bonding locations in a holding member with a chip support surface. Then, preformed bonding material is provided at the bonding locations, the preformed bonding material comprising a non-collapsible conductive metal lower portion for providing non-organic standoff height during the bonding process and a reflowable tin cap upper portion for connecting conductive elements of a leadframe with the chip bonding locations. The conductive elements of a leadframe are then aligned with corresponding bonding locations on the semiconductor chip, and the leadframe conductivo elements are moved toward the chip bonding locations so that the bonding material is arranged between the conductive elements and the chip bonding locations. A furnace bond heating process is then used for heating the bonding material to a point of reflow so that all of the conductive elements are bonded to the bonding material tin cap upper portions and the tin cap upper portions are alloyed to the non-collapsible lower portions. A further step comprises cooling the bonding material and the leadframe conductive elements.

Yet another problem within the field of electronic component packaging involves the manner of connecting leadframe conductive elements to variously spaced next levels of packaging. It is quite common for manufacturers of conductive leadframes, such as tab leadframes, to design different leadframes to match differently pitched printed circuit board footprints. However, prior art leadframes do not have structure enabling the leadframes to be used with only slight modification with differently pitched next level of packaging bond site patterns. Therefore, what has been needed has been an efficient and variable pitch tab leadframe assembly as partially shown in the fragmentary view of Figure 12.

Referring to Figure 12, a fragm ntary view of a variable pitched tab leadframe assembly 103 is illustrated in which a plurality of substantially id ntical leadframe assembly segments 104 are shown

each comprising patterned conductive elements 107 for transmitting input and output signals to bonding locations 110 on an electronic device. Variable pitch tab leadframe assembly 103 also comprises means for providing a variable pitch to conductive elements 107 to accommodate a plurality of standard pitch bond site printed circuit board footprints, such as footprints designated by JEDEC standards. Figure 12 shows a fragment of a typical tab leadframe assembly according to the variable pitch leadframe assembly invention and may be appreciated more fully in the context of Figure 13 which illustrates, in dotted lines, the relative relation of the fragment of Figure 12 when combined with other fragments to form a complete representative outline of a typical variable pitch tab leadframe assembly 103 positioned preferably as one of a plurality of such leadframe assemblies on a sprocketed tape 112. In Figures 12 and 13, a central region labelled 116 represents the area in which a die, a semiconductor chip, or the like, is placed for interconnection with variable pitch tab leadframe assembly 103.

Preferred variable pitch tab leadframe assembly segment 104 comprises means for providing a variable pitch to conductive elements 107, conductive elements 107 each comprising a first end portion 120 arranged for connection with a semiconductor chip package located in area 116. Each conductive element also comprises a second end portion 123, the location of which is selected by the manufacturer, which is arranged for connection with a next level of packaging. Preferably, first end portions 120 of adjacent conductive elements have a first pitch spacing, and second end portions 123 of said adjacent conductive elements have a second pitch spacing which is different than the first pitch spacing. In Figure 12, this relationship is represented by adjacent conductive elements first and second end portions labelled 120a, 120b, and 123a, 123b respectively. Variable pitch tab leadframe assembly segments 104 may comprise a plurality of parallel sections each having a pitch spacing corresponding to, for example, a JEDEC standard pitch spacing commonly used within the field of component packaging. For example, the pitch spacing between lead second end portions may be 50 mils (1.25mm), 40 mils (1.0mm), 25 mils (.625mm), 20 mils (0.5mm), or even less. However, as the number of leads increases and greater density of packaging is pursued, the pitch of packaging continues to decreas . Yet each time a different pitch is used on a package, it may require a package leadframe-to-board spacing specifically for that pitch.

Thus, this variabl pitch tab leadfram invention provides leadframe assembly segments 104 which comprise conductive elements 107 for connection with a package such that the package may be connected to variously pitched next levels of packaging, and vice versa. This may be accomplished by taking a tightly pitched package and attaching a leadframe to it that has and relies on the tab design to change the leadframe-to-board pitch. Tab leadframe assembly segment 104 preferably comprises interconnect sites which are fanned out along each conductive element to various desired pitches. This permits the chip manufacturer to provide a packaged device to a variety of users depending upon the user's sophistication in bonding devices to next levels of packaging using tight pitches. In other words, one size of variable pitch tab leadframe assemblies 103 may be used on many differently pitched printed circuit boards and package arrangements by cutting conductive elements 107 for desired pitch lengths at second ends 123 from a plurality of preexisting second end pitch patterns on conductive elements 107. This results in substantial savings in that manufacturers do not have to tool new leadframes and packages for each different board or user requirement. It is to be understood that pitch spacing greater than or less than those exemplary pitch spacings indicated above are envisioned within the scope of this invention, as is the number of parallel sections on conductive elements 107 for achieving numerous different pitches.

Figure 12, therefore, illustrates a variable pitch tab leadframe assembly 103 for providing connection between a semiconductor chip package, which would be located in area 116, and a next level of packaging, which would be located in an area generally designated 126 corresponding to a printed circuit board or the like. Variable pitch tab leadframe assembly 103 also preferably comprises leadframe assembly segments 104 comprising a plurality of patterned conductive elements 107 for transmitting input and output signals to bonding locations on an electronic device. Variable pitch tab leadframe assembly 103 also preferably comprises means for providing a variable pitch pattern to conductive elements 107 each comprising a first section 130 and a second section 132 in which adjacent conductive elements are arranged in parallel, and a third section 133 in which adjacent conductive elements 107 are in non-parallel, the first and second sections being connected by the third section. Also, each conductive element 107 preferably comprises a first end portion 120 for connecti n with a semiconductor chip package ahd a second end portion 123 for connection with a next level of packaging. It is to be understood that second end portions 123 may be located at various lengths or pitches, as shown in Figures 12-16. First end portions 120 of adjacent conductive elements 107 preferably have a first pitch spacing and sec-

ond end portions 123 of said adjacent conductive elements 107 have a second pitch spacing which is different than the first pitch spacing. Thus, the pitch spacing on preferred variable pitch tab leadframe assembly 103 between adjacent conductive elements 107 differs between the first and second sections.

Although various pitch spacings may be utilized in a variable pitch tab leadframe assembly 103 of the present invention, first end portions 120 of adjacent conductive elements 107 are spaced at any practicable pitch. Similarly, the corresponding second end portions of adjacent conductive elements 107 may be spaced at a pitch of generally between about 5 mils(0.125mm) and 50 mils (1.25mm). It is appreciated that the next level of packaging user will determine the appropriate pitch for leadframe-to-board attach. For example, as illustrated in Figures 14-16, adjacent conductive element second end portions 123 comprise different pitches depending on where the conductive elements 107 are severed, as determined by the pitch of the bond sites at the next level of packaging. In Figure 14, second end portions 123 are shown positioned at corresponding bond pads 130 having a pitch P1. In contrast, Figure 15 illustrates a next level of packaging requirement with bond pads 140 having a pitch P2 that is different from pitch P1. Similarly, Figure 16 illustrates another packaging requirement for which a pitch P3 exists between bond pads 150. No prior art tab leadframe assembly is known or available with structure to accommodate the multiple next level of packaging pitch requirements as depicted in Figures 14-16, or more. However, variable pitch tab leadframe assembly 103 may be used for various pitch requirements with the great advantages of simplicity, material efficiency, and savings of electronic packaging time, and is thus preferred.

A method of providing a tab leadframe assembly is also provided which permits electrical connection between a semiconductor chip package and a next level of packaging comprising various steps. These steps preferably comprise providing a leadframe as shown substantially as in Figure 12 comprising a plurality of patterned conductive elements; arranging the pattern of the leadframe conductive elements to provide a first section 130, a second section 132, and a third section 134 in which adjacent conductive elements are arranged in parallel, and a fourth section 133 and a fifth section 135 in which adjacent conductive elements are arranged in non-parallel fanned relation and which provide interconnection between the first, second, and third sections. Further, the step of arranging the pattern of the leadframe conductive elements may comprise providing a plurality of first, second, and third sections so that the pitch spacing of adjacent conductive elements differs between the first, second, and third sections. Further sections may be included following the above method of manufacture.

It is to be understood that while certain embodiments of the present invention have been illustrated and described, the invention is not to be limited to the specific forms, sizes, or arrangements of parts described and shown above, since others skilled in the art may devise other embodiments still within the limits of the claims.

Claims

1. A method of providing a tab leadframe assembly which permits electrical connection to one of a plurality of differently pitched next level of packaging bond site footprints the method characterised by:

a) providing a variable pitch tab leadframe assembly (103) comprising a plurality of patterned conductive elements (107);

b) arranging the pattern of the leadframe conductive elements to provide a first section (130), a second section (132), and a third section (134); each section comprising adjacent conductive elements (107) arranged in parallel and with each section comprising pitch spacing (P1, P2, P3) that is different from the other sections; and

c) positioning a leadframe conductive element fourth section (133) in connection with the first (130) and second (132) sections, and a fifth section (135) in connection with the second section (132) and the third section (134) so that adjacent conductive elements (107) in each of the fourth (133) and fifth (135) sections are positioned in non-parallel relation.

2. A variable pitch tab leadframe assembly (103) characterised by:

a) tape carrier material; and

b) a plurality of patterned conductive elements (107) adjacently arranged on the tape carrier material in a plurality of sections, comprising:

i) a first section (130), a second section (132), and a third section (134), each section comprising adjacent conductive elements (107) arranged in parallel and arranged with a pitch spacing (P1, P2, P3) that is different than the pitch spacing of the elements (107) in the other two sections;

ii) a fourth section (133) providing connection between the first section (130) and the second section (132), and a fifth section (135) providing connection between the second section (132) and the third section (134) so that adjacent conductive elements (107) in each of the fourth and fifth sections are positioned in non-parallel relation;

c) wherein the variable pitch tab leadframe assembly (103) permits electrical connection between a semiconductor chip package (126) and one of a plurality of differently pitched next level of packaging bond sites.

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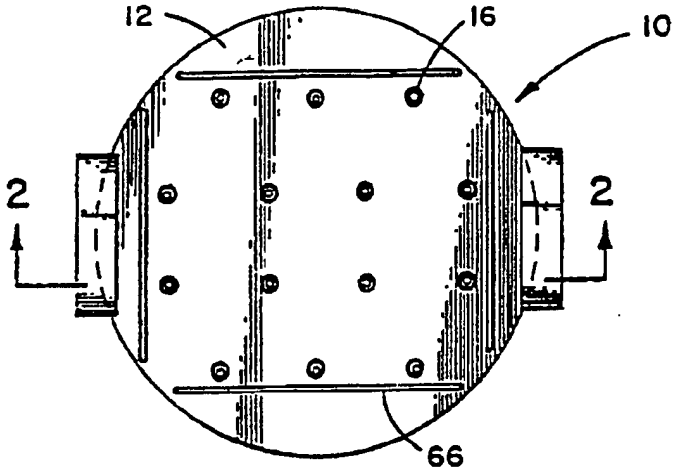


FIG. 1

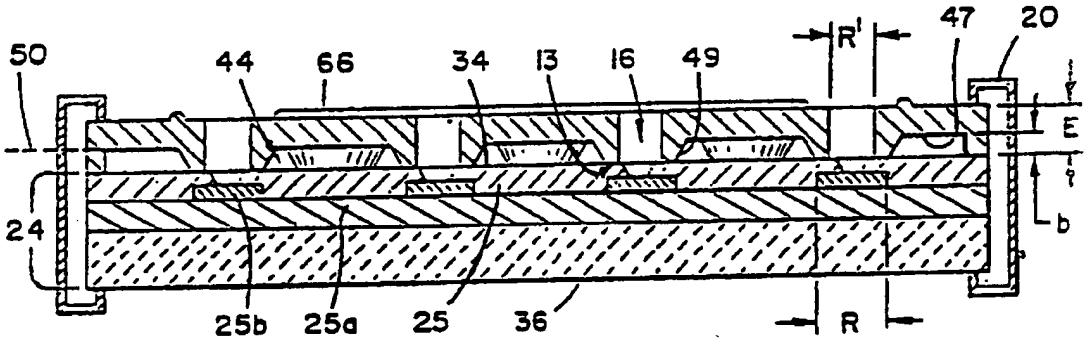
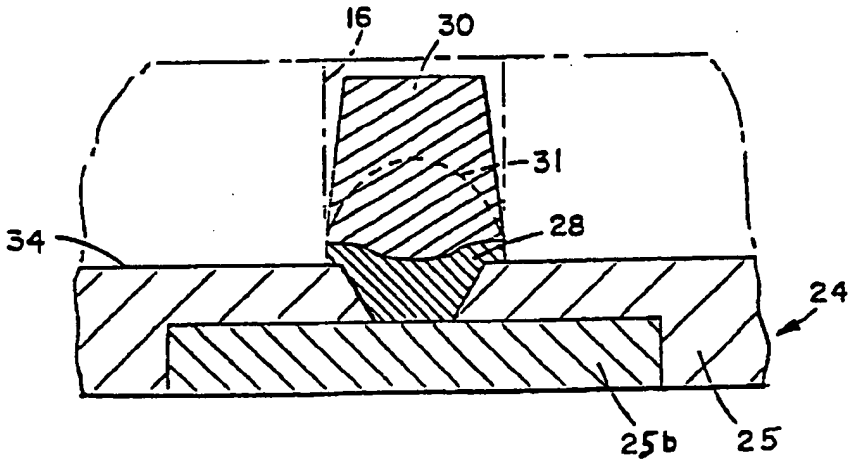


FIG. 2



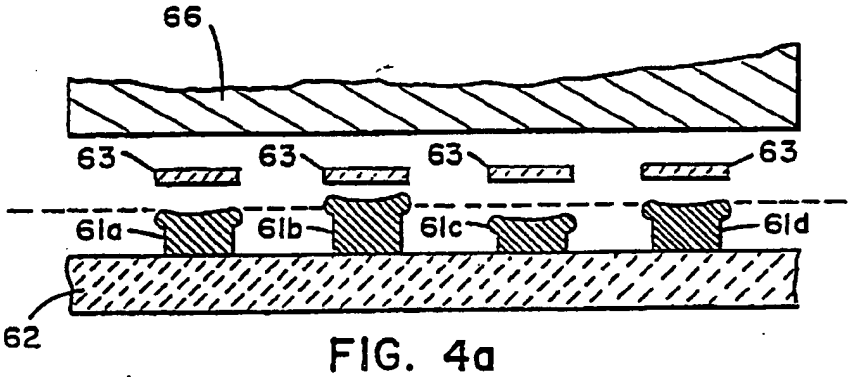


FIG. 4a

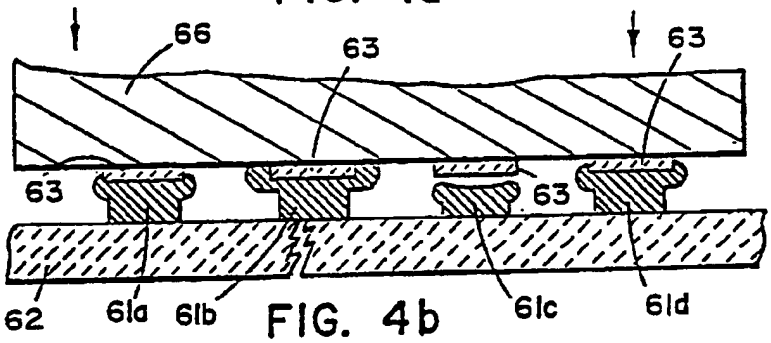


FIG. 4b

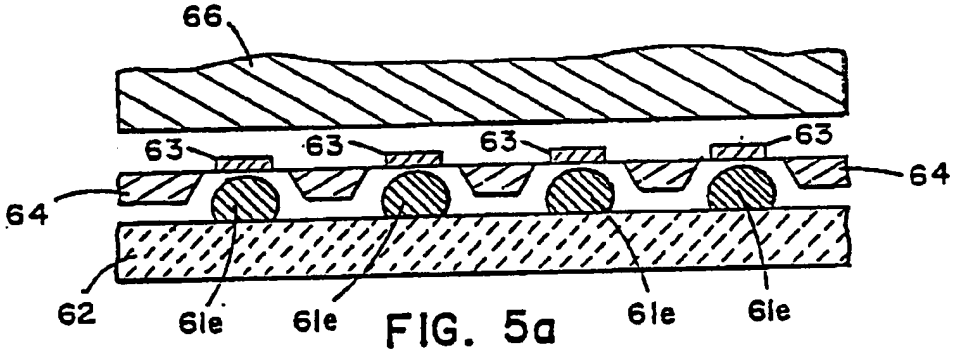


FIG. 5a

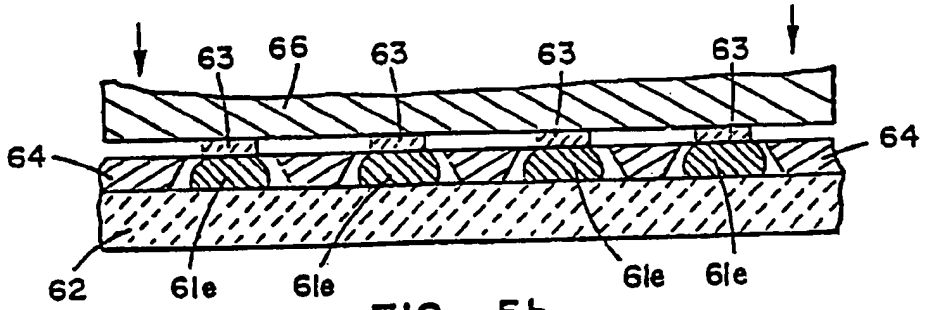


FIG. 5b

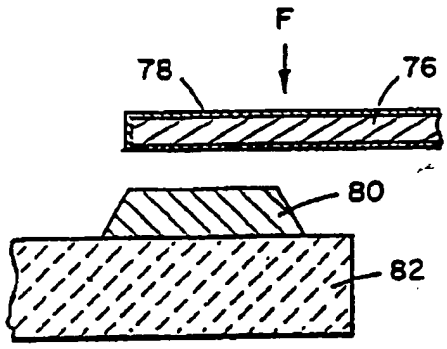


FIG. 6 (PRIOR ART)

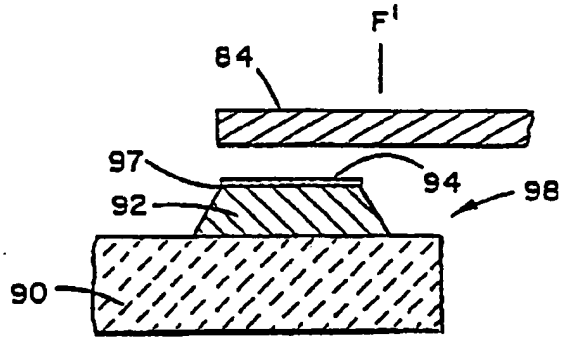


FIG. 7

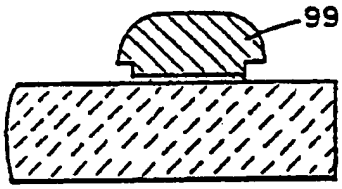


FIG. 8 (PRIOR ART)

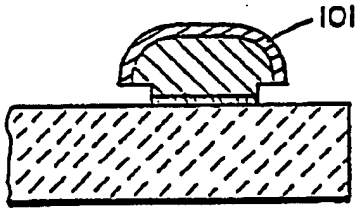


FIG. 9

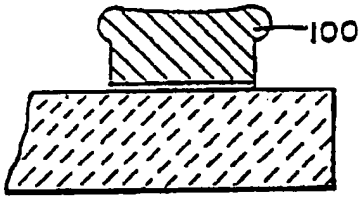


FIG. 10 (PRIOR ART)

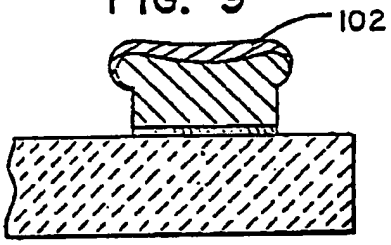


FIG. 11

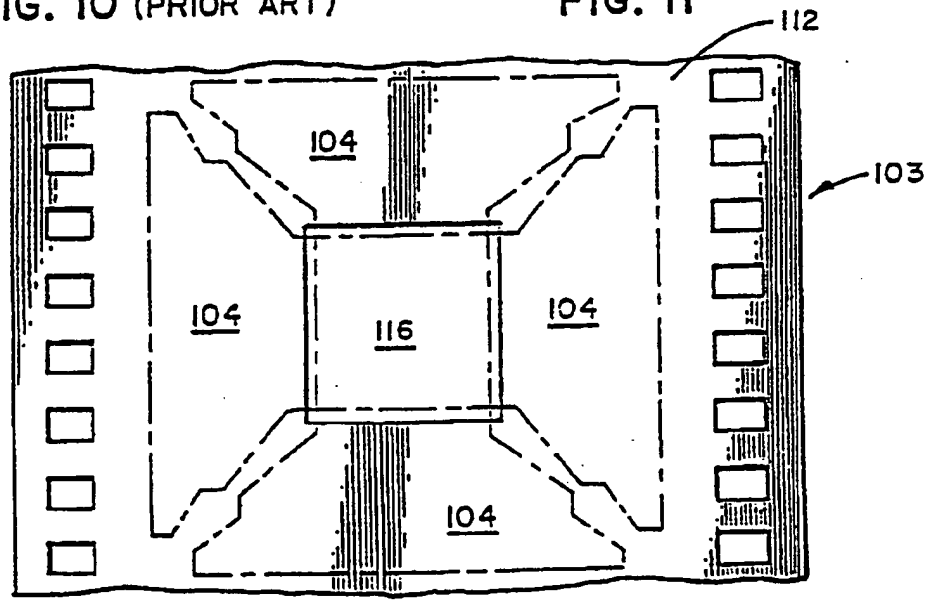
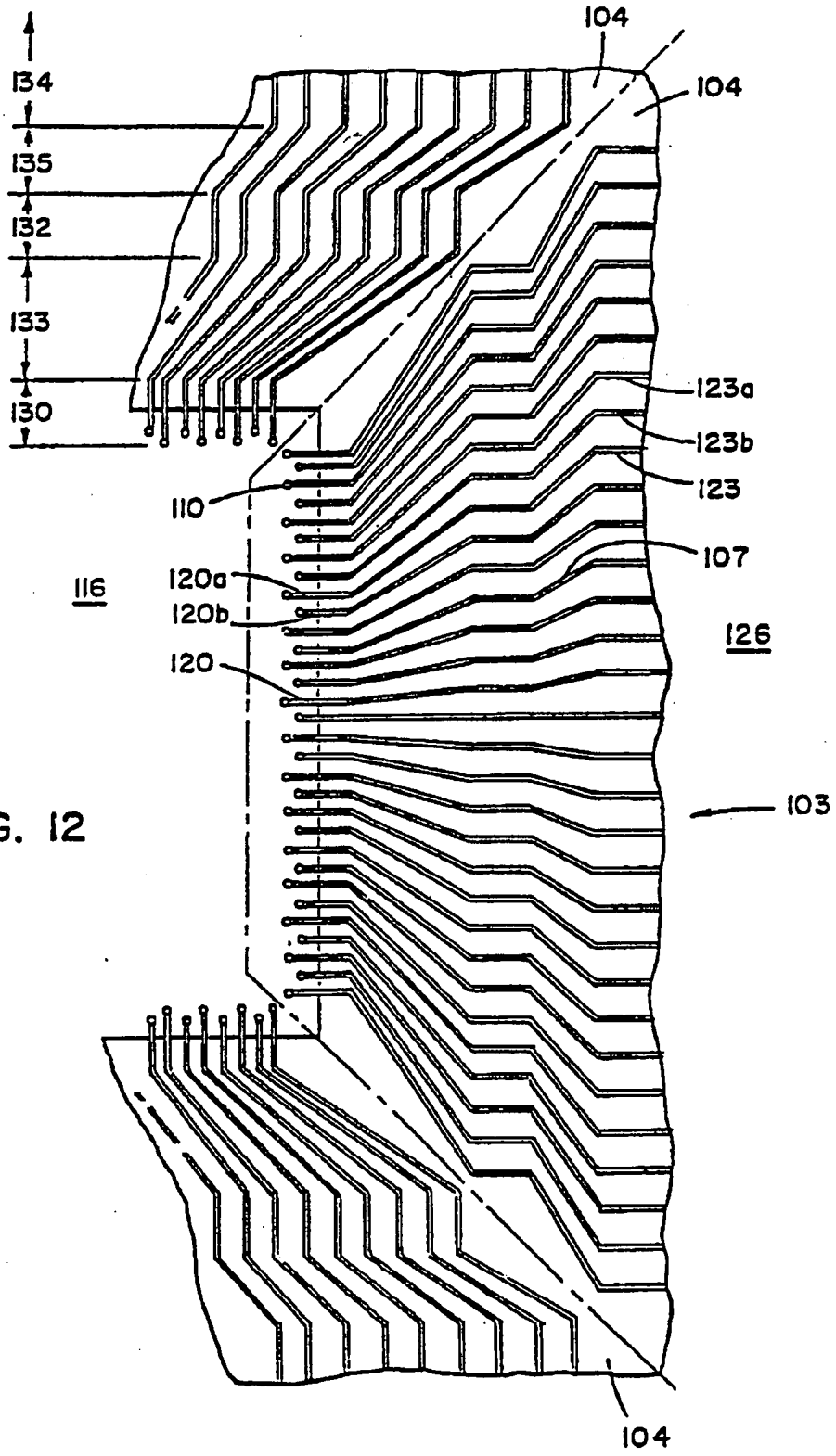


FIG. 13


104
104
134
135
132
133
130
123a
123b
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107
116
120a
120b
126
120
103
104

FIG. 12

FIG. 14

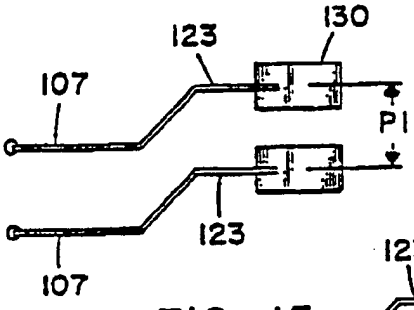


FIG. 15

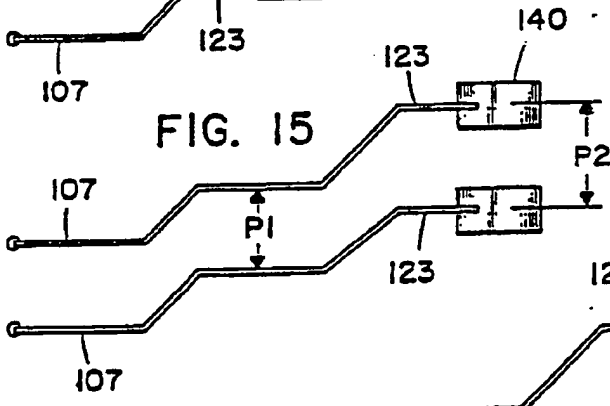
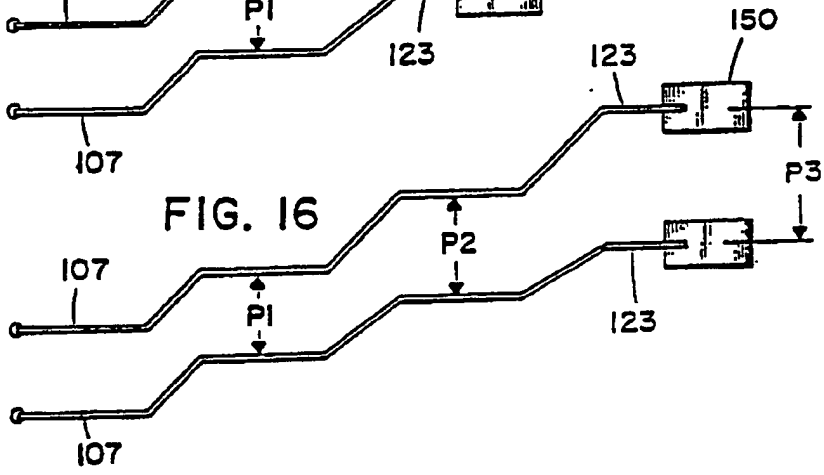
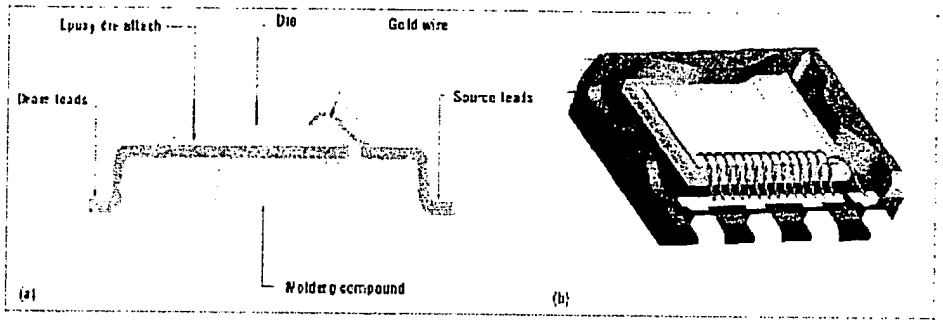


FIG. 16



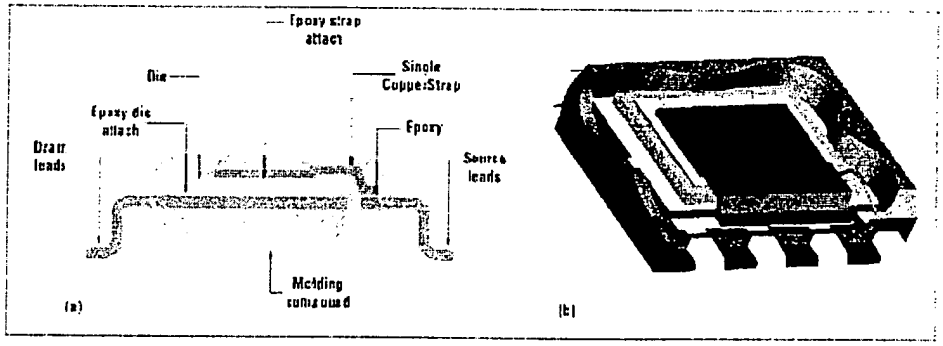
particular interest to buck-converter designers.

To date, MOSFET makers have managed to push silicon-die resistance into the single-digit milliohm range. But even this doesn't suffice. As a result, designers have been forced to opt for either a bigger, more expensive die in a larger package or for parallel arrays of less expensive devices that serve to reduce resistance, while spreading any generated heat around the board. Designs using either or both of these methods have been able to squeeze up to 10 A at 1.6 V from an input range of 10 to 21 V out of an SO-8 package. With upcoming designs looking for 15 A at 1.3 V from similarly sized or smaller packages, though, it becomes apparent that a new approach is necessary.



1. Traditional MOSFETs use wirebonding to attach the die to the source lead and the pc board (a). The wirebonds and top-metal-sheet resistance contribute about 90% of package resistance (b). Also, gold bonds are susceptible to voids, intermetallic formations, and parasitic inductance at high frequencies.

IR looked closely at all the elements that contribute to device resistance ***(Fig. 1a and b)***. In doing so, researchers realized that the wirebonds and top-metal-sheet resistance together contributed about 90% of the overall package resistance. The fourteen 2-mil gold wirebonds alone, already a maximum number for an SO-8 package, contributed about 1.1 m□. Replacing the wires with the CopperStrap reduced this to 0.11 m□ ***(Fig. 2a and b)***.



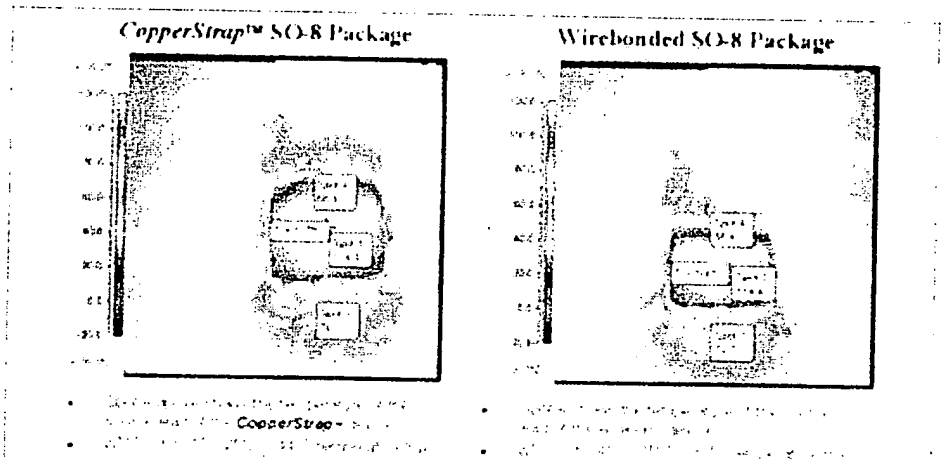
2. Replacing the fourteen 2-mil gold wirebonds (the maximum an SO-8 package can handle) with the CopperStrap reduced the die-source resistance from 1.1 m□ to 0.11 m□ (a). The top-metal resistance of the die shrank from 1.5 m□ to about 0.7 m□ (b).

The top-metal resistance of the die isn't normally taken into account when calculating package resistance, as it isn't considered to be part of the package. But depending on the location of the wirebonds on the top metal, 4 μm of aluminum could contribute as much as 1.5 m□. Placing the CopperStrap over most of the die's top surface provides a low-resistance parallel path, thereby reducing

the 1.5 m□ to about 0.7 m□. That's a 61% reduction. If the die's top metal is much less than 4 μm, overall resistance savings could be even greater.

The implications for thermal management are even more interesting. Most of the heat from a power device in an SO-8 package is removed through a plate that forms the drain-lead connection on the back of the die. It's then conducted out to the copper in the pc board. Covering up to 70%, the top surface of the die with the copper sheet provides two thermal-dissipation avenues. The first is through the source leads to the pc board. The second takes advantage of the fact that the copper strap is routed closer to the top of the mold compound encapsulant than the traditional wirebonded solution. This allows heat to escape through radiation from the top surface of the package.

To get a better idea of how the CopperStrap theory plays out in practice, a thermograph was taken of two power MOSFETs in an SO-8 package ***(Fig. 3a and b)***. As can be seen from the image, the CopperStrap device does a much better job of conducting heat to the source leads, thereby taking it away from the die itself. This allows the device to deliver more power for a given device junction temperature.



3. A thermograph of two power MOSFETs in an SO-8, one with the CopperStrap (a) and one with wirebonding (b), shows how the CopperStrap device conducts more heat to the source leads, taking it away from the die. This allows the device to deliver more power for a given device junction temperature.

The CopperStrap's thermal capabilities can be put to maximum use in applications such as synchronous buck converters. Here, the low-side MOSFET's source connection is at ground potential. By increasing the thickness and area of the copper ground plane on the pc board, more heat can be pulled out of the die through the source pins.

CopperStrap has an extra advantage in buck converters. Its reduced source inductance is a result of wire elimination. But the degree to which performance has been improved hasn't been quantified yet.

On the reliability end, getting rid of the gold wire eliminates two major problems. First is wirebond cratering. It occurs when silicon fractures as a result of unoptimized wirebond parameters--the bonding force, as well as the intensity and duration of ultrasonic power. Cratering can't be detected reliably at final test. Therefore, it usually appears during reliability testing or in the field.

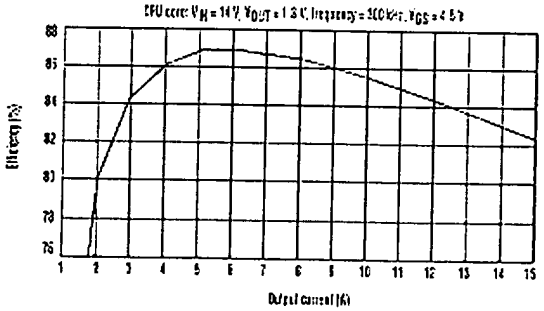
CopperStrap also puts an end to "purple plague." When gold is combined with an aluminum top metal, there's a risk of intermetallic formations. When exposed to high temperatures and/or small levels of

contaminants, the formations can be accelerated and can result in Kirkendall voids. These act in series with overall package resistance and can even result in complete open conditions. Purple plague can't be detected at final test, either. And once present, it can be very difficult to contain or control.

Other materials issues come into play. While copper is compatible with silver-filled epoxy and aluminum top metal, properties of the molding compound and silver-filled epoxy must be selected to optimize thermal, mechanical, and moisture resistance. Also,copper's expansion rate is different from that of gold wires. This has to be taken into account, especially when exposed to high solder-reflow temperatures and temperature cycling. The shape and features of the strap play a key role in how well stresses are distributed under these conditions.

KEY DEVICE PARAMETERS		
Parameter	**IRF7809**	**IRF7811**
V_{DS}	30 V	30 V
R_{DS}(ON)TYP	6m□	9m□
$Q_{G\,(TYP)}$	63 nC	18.2 nC
$Q_{SWITCH\,(TYP)}$	16.2 nC	5.8 nC
$R_{TH\,J\,LEAD\,(MAX)}$	20°C/W	20°C/W
$R_{TH\,J\,AMB\,(MAX)}$	35°C/W	35°C/W
Qswitch = $Q_{GS}2 + Q_{GD}$, where $Q_{GS}2$ = post gate-source threshold charge.		

CopperStrap is available in a dual chipset version: the high-side IRF7809, which uses PlanarFET technology, and the low-side TrenchFET-based IRF7809. Key performance specifications for these devices are shown **in the table**. The combination's ability to achieve efficiencies of up to 87% at 14 V_{IN}/1.3 V_{OUT}/6 A also is shown ***(Fig. 4)***. Efficiency falls off to about 83% at 15 A.



4. To date, the CopperStrap is capable of achieving efficiencies of up to 87% at 6 A. The efficiency falls off to about 83% at 15 A.

Cost per device is an extremely important facet of any product change or modification. In this case, there's no cost barrier, as the same manufacturing techniques and tooling can be used with minor adjustments. The only additional operation is the copper-strap placement, which can actually be incorporated into the existing die-attach operation.

Price And Availability

The IRF7809 and IRF7811 will be available in June as a chipset for $1.25 each per pair in 100,000-unit

quantities.

International Rectifier, Processor Power Group, 233 Kansas St., El Segundo, CA 90245; contact Carl Smith (310) 252-7968; fax (310) 252-7167; e-mail: csmith1@irf.com.

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Leadless Leadframe Package (LLP)

National Semiconductor
Application Note 1187
October 2002

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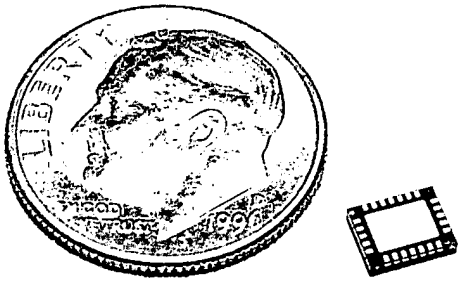

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FIGURE 1. 24 Pin LLP

Introduction

The Leadless Leadframe Package (LLP) is a leadframe based chip scale package (CSP) that may enhance chip speed, reduce thermal impedance, and reduce the printed circuit board area required for mounting. The small size and very low profile make this package ideal for high density PCBs used in small-scale electronic applications such as cellular phones, pagers, and handheld PDAs. The LLP has the following advantages:

- Low thermal resistance
- Reduced electrical parasitics
- Improved board space efficiency
- Reduced package height
- Reduced package mass

Package Overview

KEY ATTRIBUTES

- Construction of the LLP is Illustrated in *Table 1*, *Figure 2*, and *Figure 3*.
- Terminal contacts:
  - — The contact pads (or solder pad) are located peripherally in single row, dual rows or in array format depending on the specific number of pins and body size.
  - — For certain specific applications the packages are incorporated with common power and/or ground pins as illustrated in *Figure 7*.
  - — All LLP contacts are plated with 85Sn/15Pb solder for ease of surface mount processing.
  - — All Lead-Free LLP contacts are plated with matt tin solder for ease of surface mount processing.
- Printed Circuit Board (PCB) footprint:
  - — National recommends a one-to-one correlation between the PCB land patterns and the package footprint.
  - — Soldering the exposed die attach pad (DAP) to the PCB provides the following advantages:
    - Optimizes thermal performance.
    - Enhances solder joint reliability.
    - Facilitates package self alignment to the PCB during reflow.
- The LLP is offered in either dual-in-line (DIP) or quad configuration.
- Coplanarity is not an area of concern for this package.
  - — All LLP contacts are flush with the bottom of the package.
- Moisture Sensitivity Level (MSL).
  - — All LLP packages are MSL 1 without the downbond. Specific package MSL can be confirmed via product application sheets.
  - — MSL of specific applications, requiring large packages, may vary depending on die size, exposed DAP design, and number of downbonds.

TABLE 1. Elements of the 24, 44 and 56 pin LLP

	24 Pin	44 Pin	56 Pin
Package Dimensions	5 x 4 x 0.8 mm	7 x 7 x 0.8 mm	9 x 9 x 0.8 mm
PCB Footprint Area (mm^2)	20	49	81
Standard	JEDEC	JEDEC	JEDEC
Pitch	0.5 mm	0.5 mm	0.5 mm
Weight	0.047 grams	0.104 grams	0.208 grams
Lead Frame	Copper	Copper	Copper
Lead Finish	Sn/Pb	Sn/Pb	Sn/Pb
Typical Thermal Resistance θ_{JA} (Note 1)	33°C/W	20°C/W	27°C/W (Note 2)

Note 1: The typical data reported are measured values at still air and 1 watt input power using four layer FR4 substrate with Vias and copper thickness of 2.0/1.0/1.0/2.0 oz.

Note 2: Package option with limited exposed pad size due to incorporations of ground and power rings.

Package Overview (Continued)

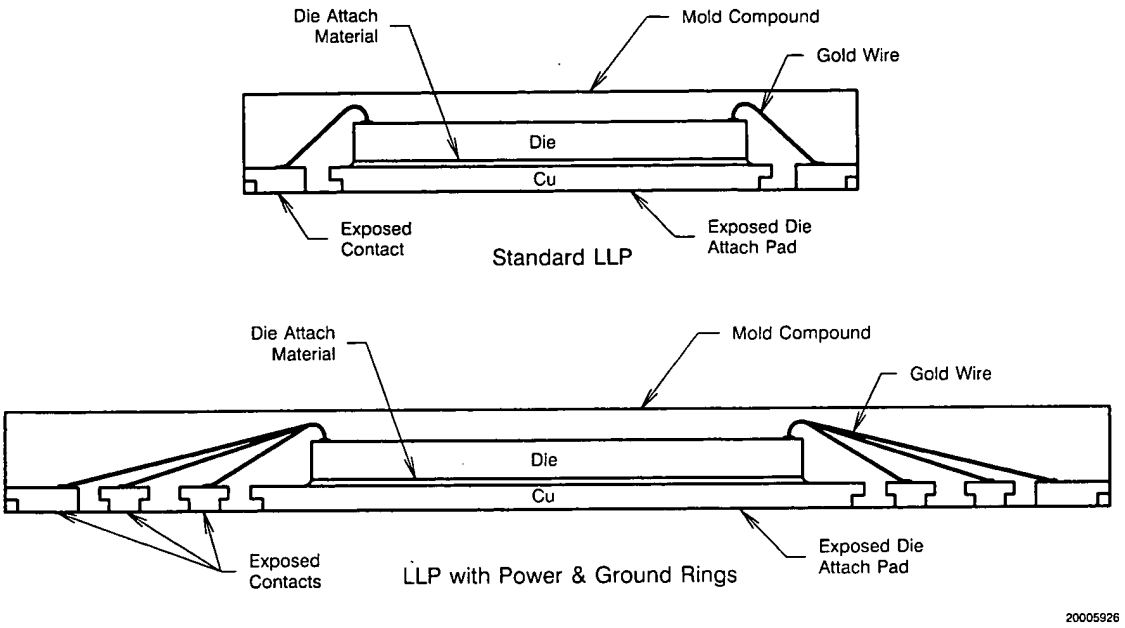


FIGURE 2. Construction of LLP

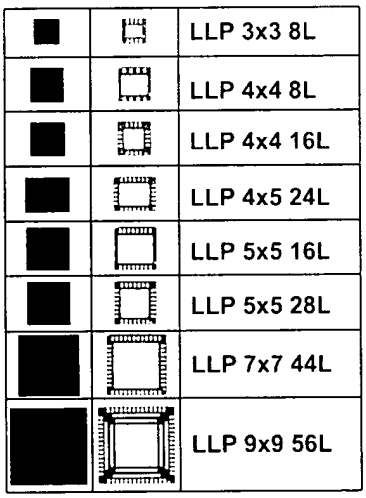


FIGURE 3. Examples

Package Overview (Continued)

PACKAGE OFFERING

Pin Count	Body size (mm)	Pitch (mm)	Max. Die Size (mm) (Note 5)	MKT DWG	MBS AD#	L/F Dwg #	QUAD/DIP (Note 4)	θ_{JA} (°C/W) (Note 3)
6	2.2 x 2.5	0.65	1.04 x 1.27	ldb06a	ldb006AA	36-1058-01	DIP	NA
6	2.92 x 3.29	0.65	1.45 x 1.85	lde06a	lde006AA	36-1056-01	DIP	NA
6	3.0 x 4.0	0.8	1.85 x 2.15	ldc06d	ldc006AE	36-0989-01	DIP	45.6
8	2.5 x 2.5	0.5	1.45 x 0.65	lda08b	lda008AC	36-1006-01	DIP	63.9
8	2.5 x 3.0	0.5	1.45 x 1.15	lda08c	lda008AD	36-1007-01	DIP	58.2
8	3.0 x 3.0	0.5	1.85 x 1.15	lda08a	lda008AA	36-0977-01	DIP	55.3
8	4.0 x 4.0	0.8	2.69 x 1.88	ldc08a	ldc008AA	36-0990-01	DIP	38.8
10	3.0 x 3.0	0.5	1.85 x 1.15	lda10a	lda010AA	36-1000-01	DIP	54.1
14	4.0 x 5.0	0.5	2.69 x 2.90	lda14b	lda014AB	36-1010-01	DIP	34.6
14	5.0 x 6.0	0.8	2.69 x 4.00	ldc14a	ldc014AA	36-1043-01	DIP	NA
16	4.0 x 4.0	0.5	2.13 x 2.13	lqa16a	lqa016AB	36-0978-02	QUAD	39.8
20	4.0 x 4.0	0.5	2.13 x 2.13	lqa20a	lqa020AB	36-1020-01	QUAD	38.7
24	5.0 x 4.0	0.5	2.10 x 3.10	lqa24a	lqa024AA	36-0973-01	QUAD	34.7
24	6.0 x 6.0	0.8	3.89 x 3.89	lqc24a	lqc024AA	36-1033-01	QUAD	NA
28	5.0 x 5.0	0.5	2.13 x 2.13	lqa28a	lqa028AA	36-0993-01	QUAD	30.8
32	5.0 x 6.0	0.5	2.13 x 2.13	lqa32b	lqa032AB	36-1031-01	QUAD	28.2
32	6.0 x 6.0	0.5	3.89 x 3.89	lqa32a	lqa032AA	36-1034-01	QUAD	26.4
44	7.0 x 7.0	0.5	4.00 x 4.00	lqa44a	lqa044AC	36-0976-03	QUAD	24.2
56	9.0 x 9.0	0.5	4.50 x 4.50	lqa56a	lqa056AA	36-1045-01	QUAD	NA

Note 3: 4-layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50 mm ground and power planes embedded in PCB

Note 4: DIP : Only two sides of the package have leads. QUAD: All four sides of the package have leads

Note 5: Maximum die size without downbond

PACKAGE HANDLING

The LLP is shipped in standard polycarbonate conductive carrier tape with pressure sensitive adhesive (PSA) cover tape. The LLP is shipped in 7"" reels. Samples can be shipped in carrier tape format and/or trays.

Pin Count	Body Size (mm)	Marketing Drawing	Reel S/N	Tape Carrier S/N	Tape Cover S/N	Tray S/N
6	2.2 x 2.5	ldb06a	017983	078156	025360	NA
6	2.92 x 3.29	lde06a	017983	076263	025360	NA
6	3.0 x 4.0	ldc06d	017983	075537	025360	NA
8	2.5 x 2.5	lda08b	017983	075535	025360	NA
8	2.5 x 3.0	lda08c	017983	075536	025360	NA
8	3.0 x 3.0	lda08a	017983	073104	025360	075393
8	4.0 x 4.0	ldc08a	017983	073105	025360	075391
10	3.0 x 3.0	lda10a	017983	073104	025360	075393
14	4.0 x 5.0	lda14b	070376	075538	025360	NA
14	5.0 x 6.0	ldc14a	017982	075539	025361	NA
16	4.0 x 4.0	lqa16a	017983	073105	025360	075391
20	4.0 x 4.0	lqa20a	017983	073105	025360	075391
24	5.0 x 4.0	lqa24a	017983	073106	025360	NA
24	6.0 x 6.0	lqc24a	017982	075540	025361	NA
28	5.0 x 5.0	lqa28a	070376	073896	025360	075392
32	5.0 x 6.0	lqa32b	017982	075539	025361	NA
32	6.0 x 6.0	lqa32a	017982	075540	025361	NA

Package Overview (Continued)

Pin Count	Body Size (mm)	Marketing Drawing	Reel S/N	Tape Carrier S/N	Tape Cover S/N	Tray S/N
44	7.0 x 7.0	lqa44a	017982	073456 073107(alt) 077373(alt)	030137 025361(alt)	073329
56	9.0 x 9.0	lqa56a	023815	076519	025361	073320

JEDEC REGISTRATIONS

- Quad LLP Packages: MO-220
- Dual-in-line LLP Packages: MO-229

PCB Design Recommendations

NSMD VS. SMD LAND PATTERN

Two types of land patterns are used for surface mount packages: (1) Non-Solder Mask Defined Pads (NSMD) and (2) Solder Mask Defined Pads (SMD). NSMD has an opening that is larger than the pad, whereas SMD pads have a solder mask opening that is smaller than the metal pad. *Figure 4* Illustrates the two different types of pad geometry.

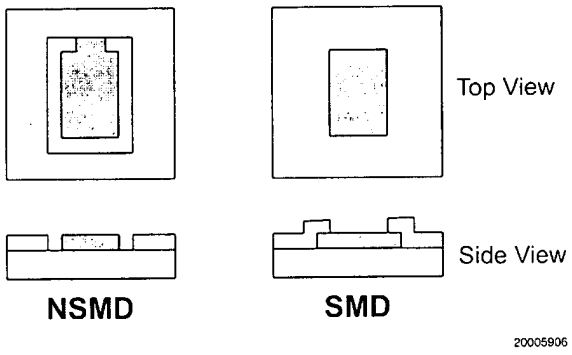


FIGURE 4. NSMD and SMD Pad Geometry

NSMD is preferred because the copper etch process has tighter control than the solder masking process. Moreover, the smaller size of the copper pad in the NSMD definition facilitates escape routing on the PCB when necessary.

NSMD pads require a ±0.075 mm (3 mils) clearance around the copper pad and solder mask this avoids overlap between the solder joint and solder mask and account for mask registration tolerances.

SMD pad definition can introduce stress concentration points near the solder mask on the PCB side. Extreme environmental conditions such as large temperature variations may cause fatigue that leads to cracked solder joints and reliability problems.

For optimal reliability, National recommends a 1:1 ratio between the package pad and the PCB pad for the LLP. If probing of signal pad is required, it is recommended to design probe pads adjacent to signal pads as shown in *Figure 5*. The trace between the signal pad and the probe pad must be covered by solder mask such that the requirement of 1:1 ratio of package pad to PCB pad is not violated. See *Figure 6* for PCB pad recommendations.

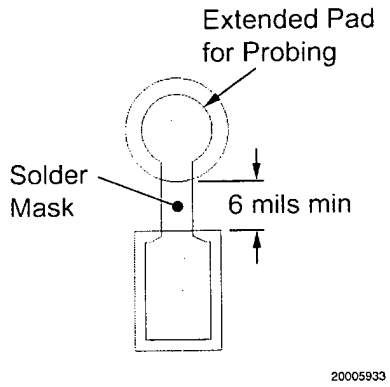
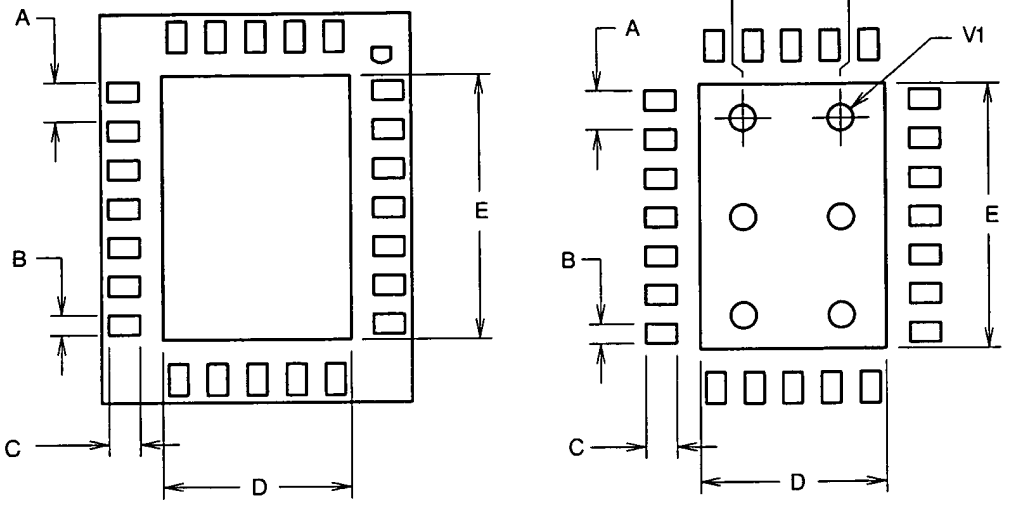


FIGURE 5. Recommended Pad Design for Probing

PCB Design Recommendations (Continued)



LLP Package Outline

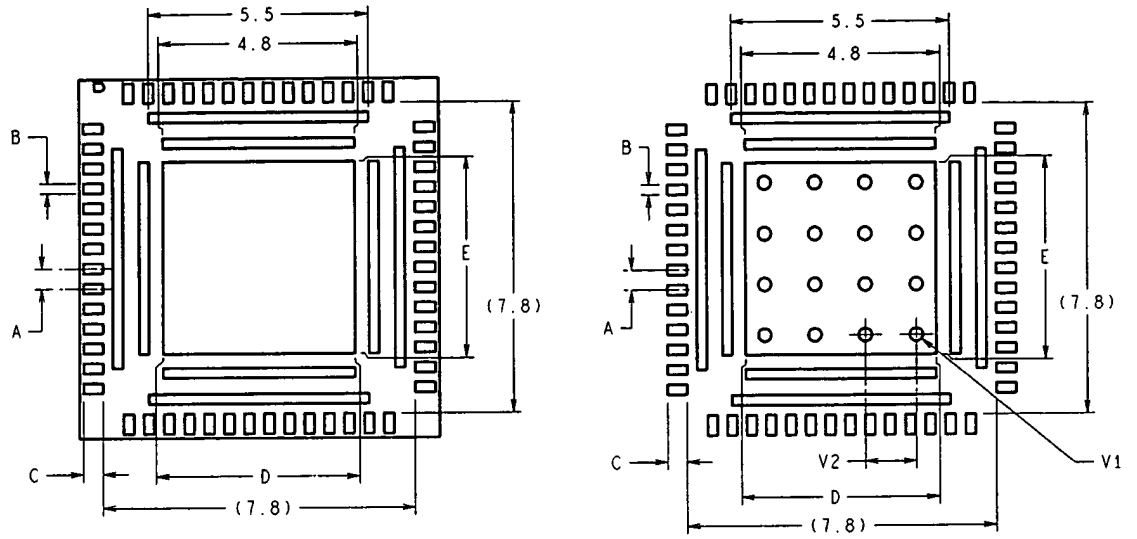
PCB Outline

20005907

Dimensions A, B, C, D, and E of PCB are 1:1 ratio with package pad dimensions. For specific detailed package dimensions refer to respective marketing outlines.
A - LLP Terminal Pitch
B - LLP Terminal Width
C - LLP Terminal Length
D - Exposed DAP Width
E - Exposed DAP Length
V1 - Thermal Via Diameter. Recommended 0.2 - 0.33 mm
V2 - Thermal Via Pitch. Recommended 1.27 mm

FIGURE 6. Typical Recommended Printed Circuit Board Dimensions

PCB Design Recommendations (Continued)



LLP Package Outline

PCB Outline

20005927

Number of pins	56
Package Size (mm)	9 x 9
A - LLP Terminal Pitch (mm)	0.5
B - LLP Terminal Width (mm)	0.25
C - LLP Terminal Length (mm)	0.5
D - Exposed DAP Width (mm)	4.8
E - Exposed DAP Length (mm)	4.8
V1 - Thermal Via Diameter (mm)	0.2 - 0.33
V2 - Thermal Via Pitch (mm)	1.27

FIGURE 7. Recommended Printed Circuit Board Dimensions for LLP 56 L with Ground and Power Bars.

THERMAL DESIGN CONSIDERATIONS

THERMAL LAND

The LLP thermal land is a metal (normally copper) region centrally located under the package and on top of the PCB. It has a rectangular or square shape and should match the dimensions of the exposed pad on the bottom of the package (1:1 ratio).

For certain high power applications, the PCB land may be modified to a "dog bone" shape that enhances thermal performance. The packages used with the "dog bone" lands will be a dual inline configuration. (See *Figure 8*).

PCB Design Recommendations

(Continued)

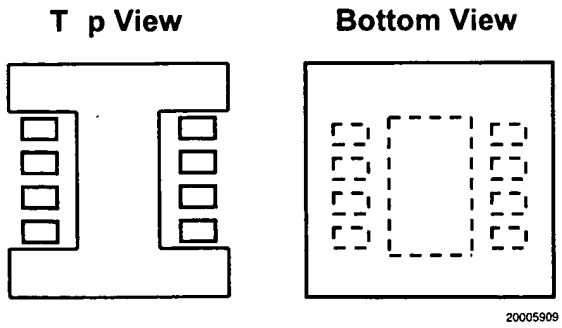


FIGURE 8. Dog Bone

THERMAL VIAS

Thermal vias are necessary. They conduct heat from the surface of the PCB to the ground plane. The number of vias is application specific and is dependent upon electrical requirements and power dissipation. A package thermal performance may be improved by increasing the number of vias. The improvement diminishes, however, as the number of vias increase. See *Figure 9.*

An array of vias with a 1.27 mm pitch is shown in *Figure 6.* The via diameter should be 0.2 mm to 0.33 mm with 1oz. copper via barrel plating. It is important to plug the via to avoid any solder wicking inside the via during the soldering process. If the copper plating does not plug the via, the thermal vias can be tented with solder mask on the top surface of the PCB. The solder mask diameter should be at least 75 microns (or 3 mils) larger than the via diameter. The solder mask thickness should be the same accross the entire PCB.

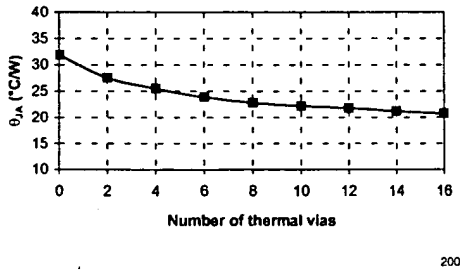


FIGURE 9. θ_{JA} vs. Number of Thermal Vias for the 44L LLP

EFFECTS OF THERMAL VOIDS

A void in the solder paste or die attach (generated during the manufacturing process) could have a direct impact on heat dissipation. The effect is not significant unless the void volume exceeds a certain percentage of the corresponding material volume (see *Figure 10*). **NOTE:** voids typically do not have an impact on reliability.

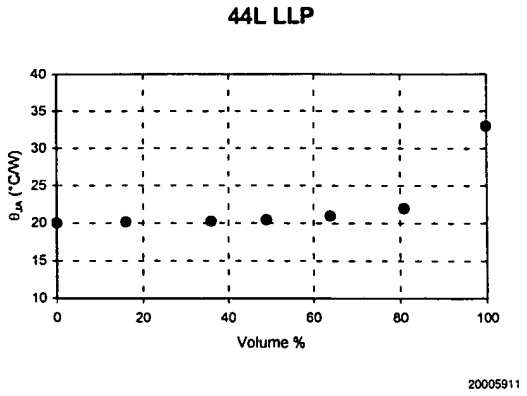


FIGURE 10. Thermal Voids Impact for the 44L LLP

THERMAL LAYERS IN THE PCB

Because of the small size and low profile, the majority of heat generated by the die within the LLP is dissipated through the exposed pad to PCB. Consequently, the PCB configuration and metal layers embedded in the PCB become important to achieving good thermal performance. In a 4-layer PCB (2 layers for signals and 2 layers for power/ground), the area of the embedded copper layer connecting to the thermal vias has significant effect on the thermal performance of the package. *Figure 11* shows simulation data of θ_{JA} vs. the embedded copper layer area for the 44L LLP. Increasing the copper layer area reduces the thermal resistance. However, in the similar manner, as the number of vias increases, the amount of thermal resistance improvement diminishes as the embedded copper area increases.

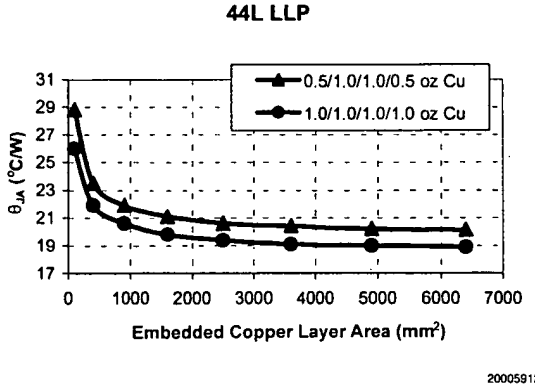


FIGURE 11. Effect of Thermal Layers on the 44L LLP's Junction-to-Ambient Thermal Resistance

SMT Assembly Recomm ndations

The LLP surface mount assembly operations include:

- PCB plating requirements
- Screen printing the solder paste on the PCB
- Monitor the solder paste volume (uniformity)
- Package placement using standard SMT placement equipment
- X-ray pre reflow check - paste bridging
- Reflow and cleaning (dependent upon the flux type)
- X-ray post reflow check - solder bridging & Voids

PCB SURFACE FINISH REQUIREMENTS

A uniform PCB plating thickness is key for high assembly yield.

- For an electroless, nickel-immersion, gold finish, the gold thickness should range from 0.05 µm to 0.20 µm to avoid solder joint embrittlement.
- Using a PCB with **O**rganic **S**olderability **P**reservative coating (OSP) finish is also recommended, as an alternative to Ni-Au.
- For a PCB with Hot Air Solder Leveling (HASL) finish, the surface flatness should be controlled within 28 micron.

SOLDER STENCIL

Solder paste deposition using a stencil-printing process involves the transfer of the solder paste through pre-defined apertures with the application of pressure. Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the LLP package is highly recommended to improve board assembly yields.

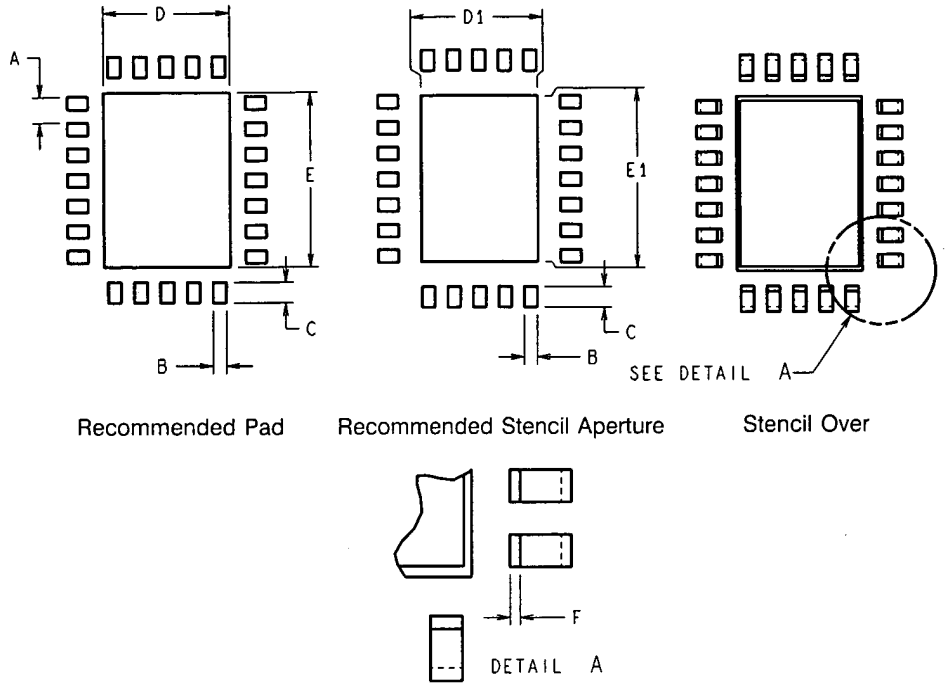
Stencils fabricated from chemical etching with elctro polished or laser cut is recommended. Tapered aperture walls (5° tapering) is recommended to facilitate paste release. Recommended stencil thickness is 127 µm. In order to prevent solder bridging the stencil aperture openings need to be modified as follows:

- The terminal contact aperture openings should be offset by 0.1 mm outward from the pads.
- For exposed pad aperture, up to 2 mm, the opening should be reduced to 95% of the corresponding PCB exposed DAP dimensions. See *Figure 12* and *Figure 13*.
- For exposed pad aperture with any side from 2 to 4 mm, the stencil opening should be split in two for any side. See *Figure 14*.
- For exposed pad aperature greater than 4 mm but without ground and power bars. See *Figure 15*.
- For exposed pad aperature greater than 4 mm with ground and power bars. See *Figure 16*.

TABLE 2. LLP Stencil Aperature Summary

Pin Count	MKT Dwg	I/O pad size	Pitch	DAP size	Stencil I/O	Aperature DAP	Dimension		
							D1	E1	H
6	ldb06a	0.25 X 0.4	0.65	1.2 X 0.75	0.25 X 0.4	*Figure 13*	1.1	0.7	N/A
6	ldc06d	0.3 X 0.5	0.8	2 X 2.2	0.3 X 0.5	*Figure 14*	0.85	0.85	0.3
6	lde06a	0.35 X 0.5	0.95	1.92 X 1.2	0.35 X 0.5	*Figure 13*	1.8	1.1	N/A
8	lda08a	0.25 X 0.5	0.5	1.8 X 1.2	0.25 X 0.5	*Figure 13*	1.7	1.1	N/A
8	lda08b	0.25 X 0.5	0.5	1.5 X 0.7	0.25 X 0.5	*Figure 13*	1.4	0.6	N/A
8	lda08c	0.25 X 0.5	0.5	1.5 x 1.2	0.25 X 0.5	*Figure 13*	1.4	1.1	N/A
8	ldc08a	0.3 X 0.5	0.8	3 X 2.2	0.3 X 0.5	*Figure 14*	1.25	0.85	0.3
10	lda10a	0.25 X 0.5	0.5	2 X 1.2	0.25 X 0.5	*Figure 13*	1.9	1.1	N/A
14	lda14b	0.25 X 0.5	0.5	3 X 3.2	0.25 X 0.5	*Figure 14*	1.25	1.35	0.3
14	ldc14a	0.4 X 0.5	0.8	4.35 X 3	0.4 X 0.5	*Figure 14*	1.925	1.25	0.3
16	lqa16a	0.25 X 0.5	0.5	2.2 X 2.2	0.25 X 0.5	*Figure 14*	0.85	0.85	0.3
20	lqa20a	0.25 X 0.5	0.5	2.2 X 2.2	0.25 X 0.5	*Figure 14*	0.85	0.85	0.3
24	lqa24a	0.25 X 0.4	0.5	3.4 X 2.4	0.25 x 0.4	*Figure 14*	1.45	0.95	0.3
24	lqc24a	0.3 X 0.5	0.8	4.2 X 4.2	0.3 X 0.5	*Figure 15*	0.5	0.5	0.3
28	lqa28a	0.25 X 0.5	0.5	3.2 X 3.2	0.25 X 0.5	*Figure 14*	1.35	1.35	0.3
32	lqa32a	0.25 X 0.5	0.5	4.2 X 4.2	0.25 X 0.5	*Figure 15*	0.5	0.5	0.3
32	lqa32b	0.25 X 0.5	0.5	4.2 X 3.2	0.25 X 0.5	*Figure 15*	0.5	0.5	0.3
44	lqa44a	0.25 X 0.5	0.5	4.3 X 4.3	0.25 X 0.5	*Figure 15*	0.5	0.5	0.3
56	lqa56a	0.25 X 0.5	0.5	4.8 X 4.8	0.25 X 0.5	*Figure 16*	0.5	0.5	0.3

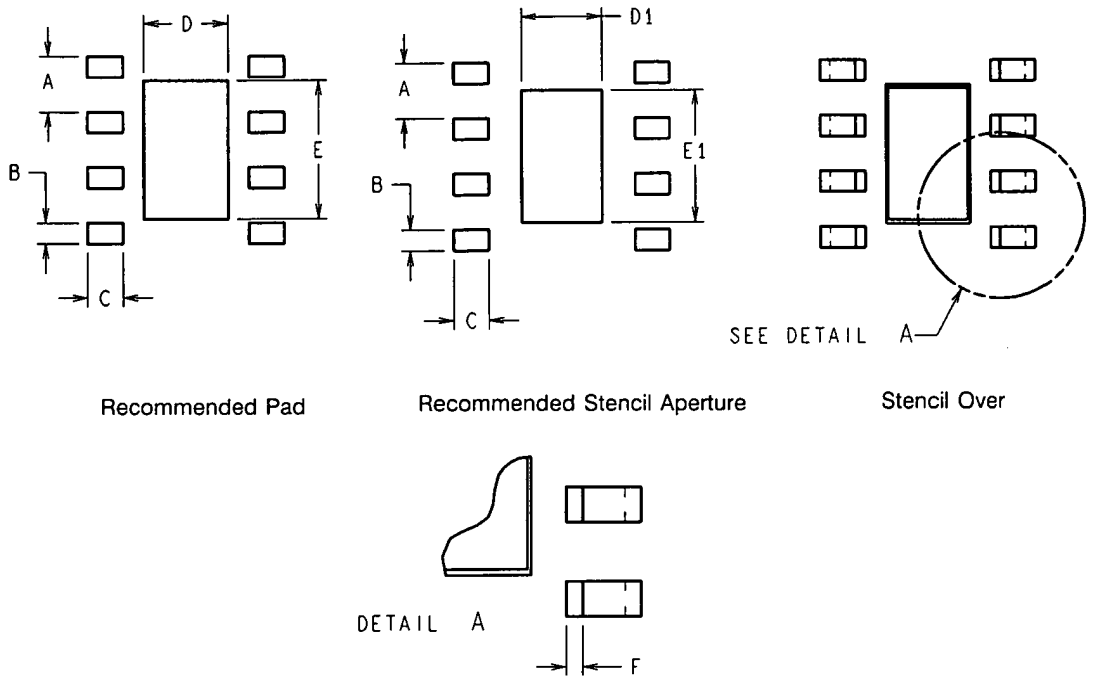
SMT Assembly Recommendations (Continued)



A, B and C of Stencil	1:1 ratio with A, B and C of PCB pad
D1	0.95 x D
E1	0.95 x E
F	0.1 mm
Note: For specific detailed package dimensions refer to respective Marketing Outlines.	

FIGURE 12. Typical Recommended PCB Dimensions vs. Stencil Aperture for Quad Packages with DAP < 2 mm.

SMT Assembly Recommendations (Continued)

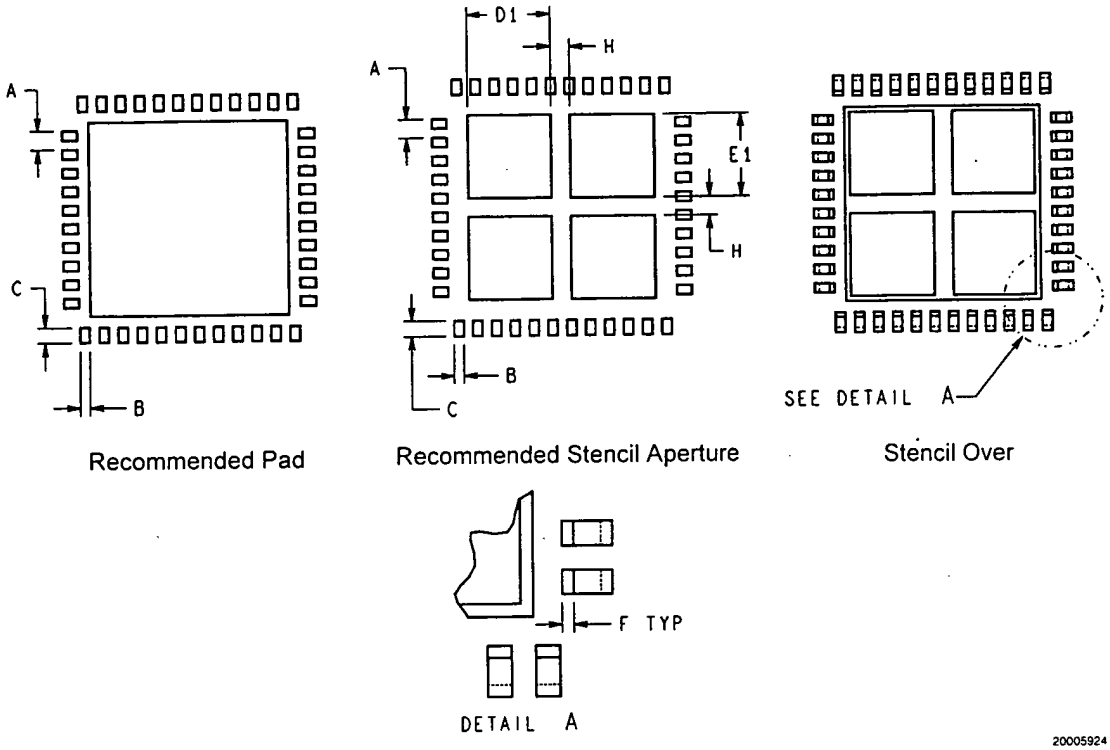


Recommended Pad | Recommended Stencil Aperture | Stencil Over

A, B and C of Stencil	1:1 ratio with A, B and C of PCB pad
D1	0.95 x D
E1	0.95 x E
F	0.1 mm
Note: For specific detailed package dimensions refer to respective Marketing Outlines.	

FIGURE 13. Typical Recommended PCB Dimensions vs. Stencil Aperture for Dual In-line Packages with DAP < 2 mm.

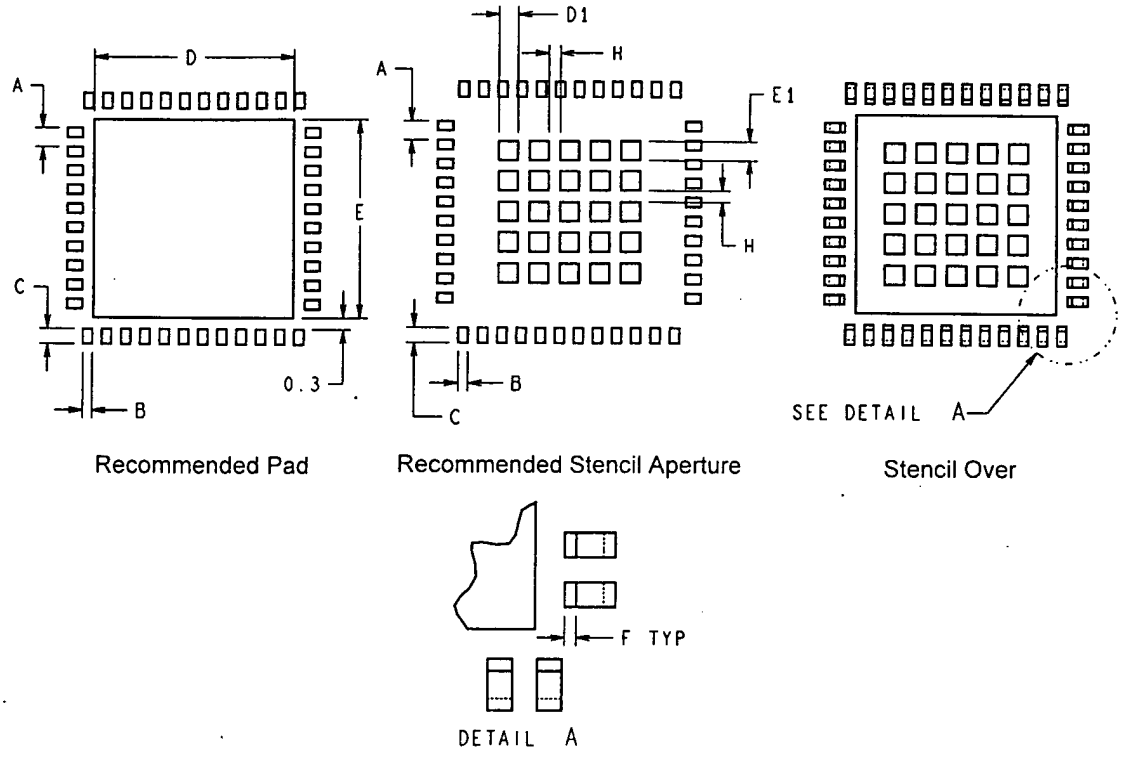
SMT Assembly Recommendations (Continued)



A, B and C of Stencil	1:1 ratio with A, B and C of PCB pad
D1	See *Table 2*
E1	
F	
Note: For specific detailed package dimensions refer to respective Marketing Outlines.	

FIGURE 14. Typical Recommended Stencil Opening for Exposed DAP from 2 mm to 4 mm.

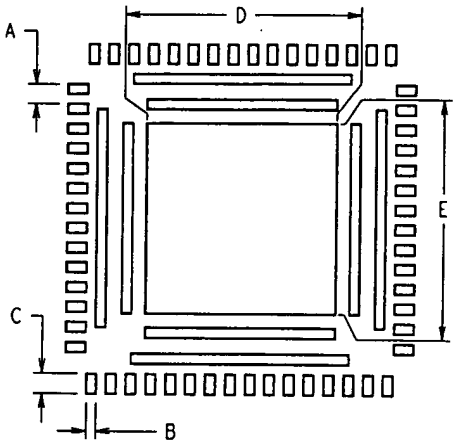
SMT Assembly Recommendations (Continued)



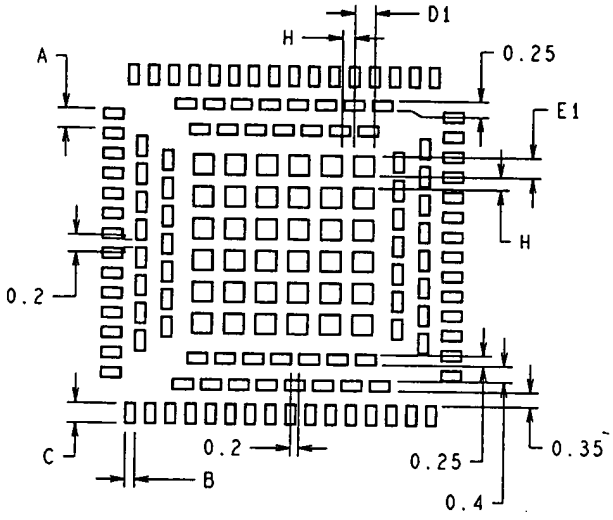
A, B and C of Stencil	1:1 ratio with A, B and C of PCB pad
D1	See *Table 2*
E1	
F	
Note: For specific detailed package dimensions refer to respective Marketing Outlines.	

FIGURE 15. Typical Recommended Stencil Opening for Exposed DAP > 4 mm on any side without Ground and Power Bars.

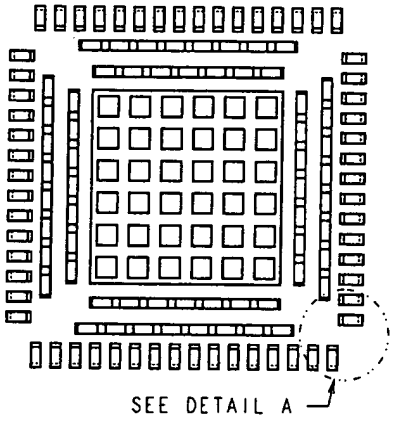
SMT Assembly Recommendations (Continued)



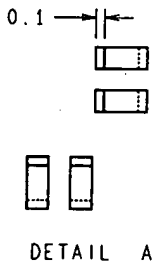
Recommended Pad



Recommended Stencil Aperture



Stencil Over



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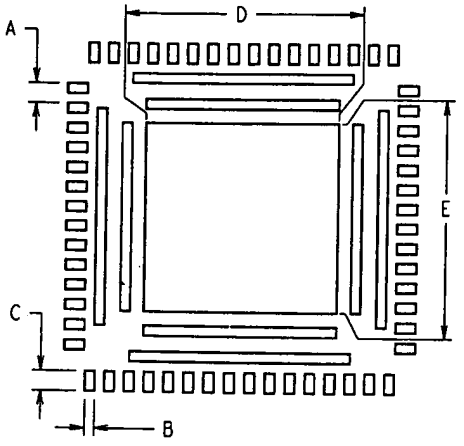
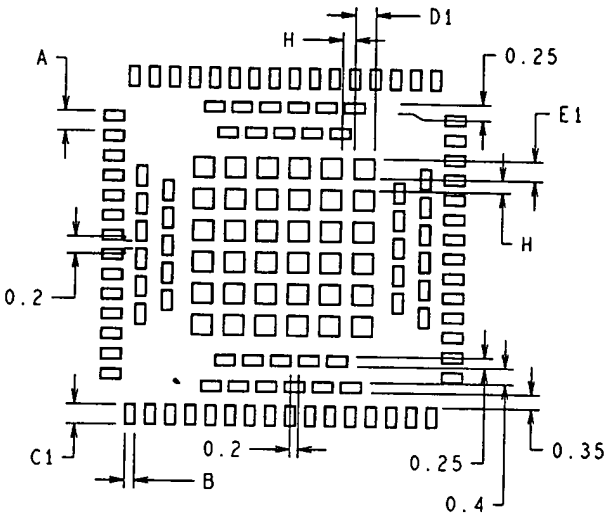
Number of pins	56
A - LLP, PCB, Stencil Terminal Pitch (mm)	0.5
B - LLP, PCB, Stencil Terminal Width (mm)	0.25
C - LLP, PCB, Stencil Terminal Length (mm)	0.5
D - LLP, PCB Exposed DAP Width (mm)	4.8
D1 - Exposed DAP Aperture Width (mm)	0.5
H - Aperture split width, centered (mm)	0.3
E - LLP, PCB Exposed DAP Length (mm)	4.8
E1 - Exposed DAP Aperture Length (mm)	0.5
F - Stencil Aperture opening offset (mm)	0.1

FIGURE 16. Typical Recommended Stencil Opening for LLP with Exposed DAP, Ground and Power Bars.

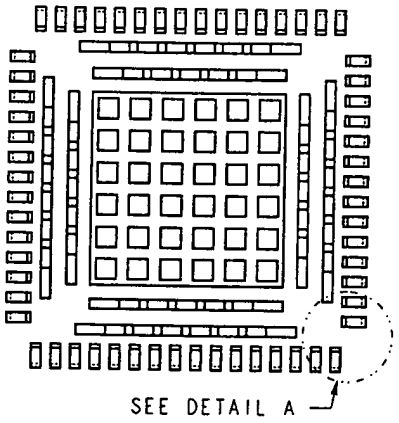
SMT Assembly Recommendations (Continued)



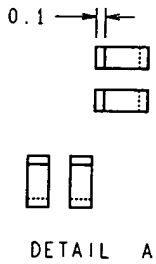
Recommended Pad



Recommended Stencil Aperture



Stencil Over



20005938

Number of pins	56
A - LLP, PCB, Stencil Terminal Pitch (mm)	0.5
B - LLP, PCB, Stencil Terminal Width (mm)	0.25
C - LLP, PCB Terminal Length (mm)	0.5
C1 - LLP Stencil Terminal Length (mm)	0.45
D - LLP, PCB Exposed DAP Width (mm)	4.8
D1 - Exposed DAP Aperture Width (mm)	0.5
H - Aperture split width, centered (mm)	0.3
E - LLP, PCB Exposed DAP Length (mm)	4.8
E1 - Exposed DAP Aperture Length (mm)	0.5
F - Stencil Aperture opening offset (mm)	0.1

FIGURE 17. Typical Recommended Stencil Opening for LLP with Exposed DAP, Ground and Power Bars for PCB with HASL Finish.

SMT Assembly Recommendations (Continued)

STENCIL OPENINGS FOR SOT23 5/6L FOOTPRINT COMPATIBLE LLP

- For the SOT23 5/6L footprint compatible LLP for which the PCB has been designed for the SOT23 package, refer to *Figure 18* for solder stencil openings.
- For new board design, it is recommended to use *Fig 13* for PCB pad and stencil openings.

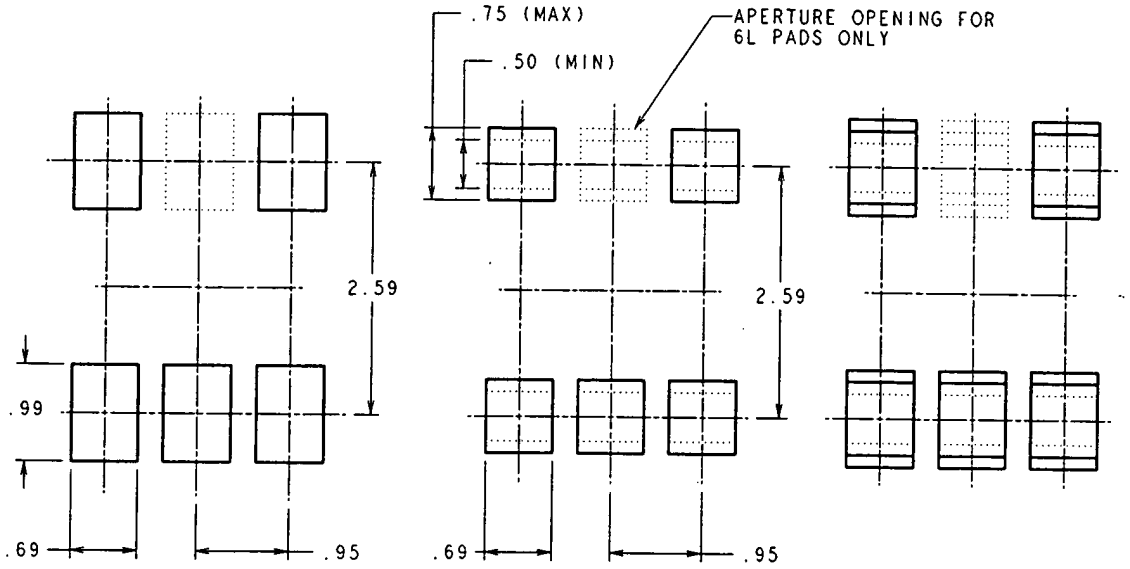


FIGURE 18. Recommended Stencil Aperture for SOT23 5/6 Lead Footprint Compatible LLP

PACKAGE PLACEMENT

LLP packages can be placed using standard pick and place equipment with an accuracy of ±0.05 mm. Component pick and place systems are composed of a vision system that recognizes and positions the component and a mechanical system which physically performs the pick and place operation. Two commonly used types of vision systems are: (1) a vision system that locates a package silhouette and (2) a vision system that locates individual bumps on the interconnect pattern. The latter type renders more accurate place but tends to be more expensive and time consuming. Both methods are acceptable since the parts align due to a self-centering feature of the LLP solder joint during solder reflow.

It is recommended to release the LLP package 1 to 2 mils into the solder paste.

SOLDER PASTE

Type 3, water soluble, no clean, and leadfree solder pastes are acceptable.

REFLOW AND CLEANING

The LLP may be assembled using standard IR / IR conv tion SMT reflow processes without any special consid ations. As with other packages, the thermal profile for sp cific board locations must be determined. Nitrogen purge recommended during solder for no-clean fluxes. The LLP qualified for up to three reflow cycles at 235°C pe (J-STD-020). The actual temperature of the LLP is a functi of:

- Component density
- Component location on the board
- Size of surrounding components

It is recommended that the temperature profile be check at various locations on the board. *Figure 19* and *Figure* . illustrate typical reflow profiles.

SMT Assembly Recommendations (Continued)

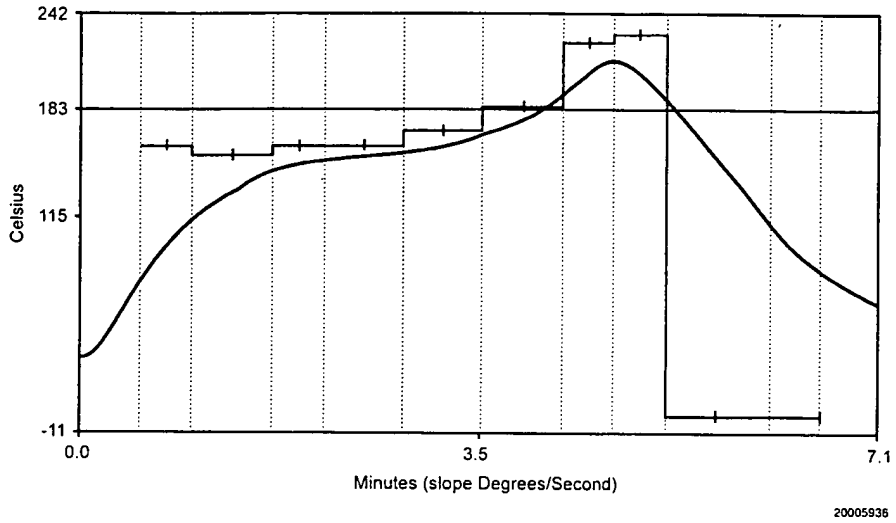


FIGURE 19. Typical Reflow Profile

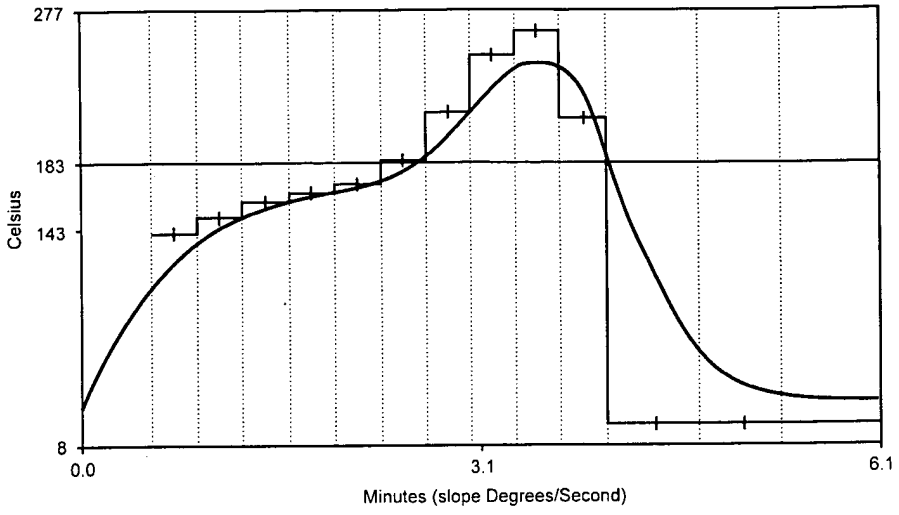
		Convection / IR
Ramp Up °C/sec (Note 8)	Maximum	4°C/sec
	Recommended	**2°C/sec** (Note 6)
	Minimum	(Note 7)
Dwell Time ≥ 183°C (Note 8)	Maximum	85 seconds
	Recommended	**75 seconds** (Note 6)
	Minimum	(Note 7)
Peak Temperature (Note 8)	Maximum	240°C
	Recommended	**215°C**
	Minimum	(Note 7)
Dwell Time Max. (within 5°C of peak temperature)	Maximum	10 seconds
	Recommended	**5 seconds**
	Minimum	1 second
Ramp Down °C/sec (Note 8)	Maximum	4°C/sec
	Recommended	**2°C/sec**
	Minimum	(Note 7)

Note 6: Will vary depending on board density, geometry, and package types. May vary depending on solder paste manufactures recommendations.

Note 7: Will vary depending on package types, and board density.

Note 8: All Temperatures are measured at the PCB surface.

SMT Assembly Recommendations (Continued)



Note : For detail settings, please refer to solder paste manufacturer's recommendation.

FIGURE 20. Typical Reflow Profile - Lead Free

SOLDER JOINT INSPECTION

After surface mount assembly, transmission X-ray should be used for **sample** monitoring of the solder attachment process. This identifies defects such as solder bridging, shorts, opens and voids. **NOTE:** voids typically do not have an impact on reliability. *Figure 21* shows a typical X-ray photograph after assembly.

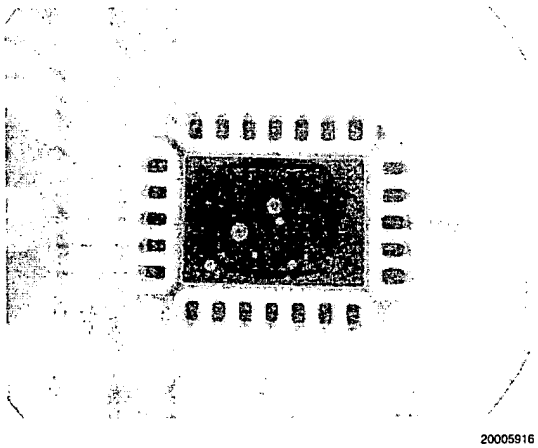


FIGURE 21. Typical X-ray after process

In the process setup, it is recommended to use side view inspection in addition to X-ray to determine if there are 'Hour Glass' shaped solder existing. The 'Hour Glass' solder shape is is not a reliable joint. 90° mirror projection can be used for side view inspection.

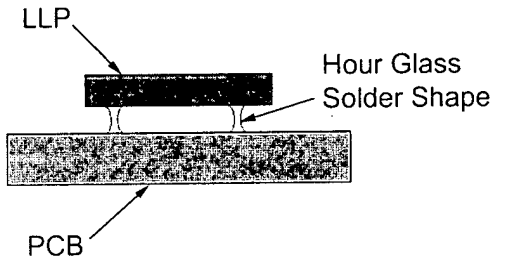


FIGURE 22.

REPLACEMENT/ REWORK

The quality of the rework is controlled by:

- Directing the thermal energy through the component body to solder without over-heating the adjacent components.
- Heating should occur in an encapsulated, inert, gas-purged environment where the temperature gradients do not exceed ±5°C across the heating zone.
- Using a convective bottom side pre-heater to maximize temperature uniformity.

SMT Assembly Recommendations

(Continued)

- Interchangeable nozzles designed with different geometries will accommodate different applications to direct the airflow path

NOTE: Standard SMT rework systems are capable of these elements.

Removal of the LLP Removing the LLP from the PCB involves heating the solder joints above the liquidus temperature of eutectic (63Sn-37Pb) solder using a vacuum gas nozzle. Baking the PCB at 125˚C for 4 hours is recommended PRIOR to any rework. Doing this removes any residual moisture from the system, preventing moisture induced cracking or PCB delamination during the demount process.

A 1.27 mm (50 mil) keep-out zone for adjacent components is recommended for standard rework processing. If the adjacent components are closer than 1.27 mm, custom tools are required for the removal and rework of the package.

It is recommended that the reflow profile used to reflow the LLP be as close to the PCB mount profile as possible. Preheat the PCB area, through the bottom side of the board, to 100˚C before heating the LLP to ensure a controlled process. Once the liquidus temperature is reached, nozzle vacuum is automatically activated and the component is removed. After removing the package, the pads may be heated with the nozzle to reflow any residual solder, which may be removed using a Teflon tipped vacuum wand.

Site Preparation Once the LLP is removed, the site must be cleaned in preparation for package attachment. The best results are achieved with a low-temperature, blade-style conductive tool matching the footprint area of the LLP in conjunction with a de-soldering braid. No-clean flux is needed throughout the entire rework process. Care must be taken to avoid burn, lift-off, or damage of the PCB attachment area. See *Figure 23.*

Solder Paste Deposition Because the LLP is a land area type package, solder paste is required to insure proper solder joint formation after rework. A 127 µm (5 mil) thick mini-stencil is recommended to deposit the solder paste patterns prior to replacement of the LLP. See *Figure 24.*

Component Placement Most CSP rework stations will have a pick and place feature for accurate placement and alignment. Manual pick and place, with only eye-ball alignment, is not recommended. It is difficult or impossible to achieve consistent placement accuracy.

Component Reflow It is recommended that the reflow profile used to reflow the LLP be as close to the PCB mount profile as possible. Preheat the PCB area, through the bottom side of the board, to 100˚C before heating the LLP to ensure a controlled process. Once the liquidus temperature is reached, the solder will reflow and the LLP will self align. *Figure 25* shows a cross section of a solder joint after rework.

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FIGURE 23. Pads After Removing Components and Cleaning

SMT Assembly Recommendations (Continued)

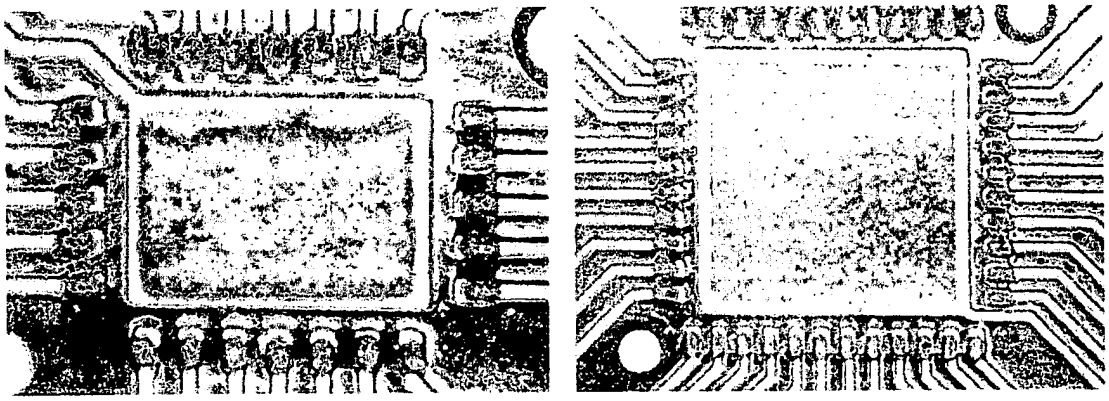

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FIGURE 24. Solder Paste Printing of LLP 24 and LLP 44 Using 127 µm (5 mil) Thick Stencil

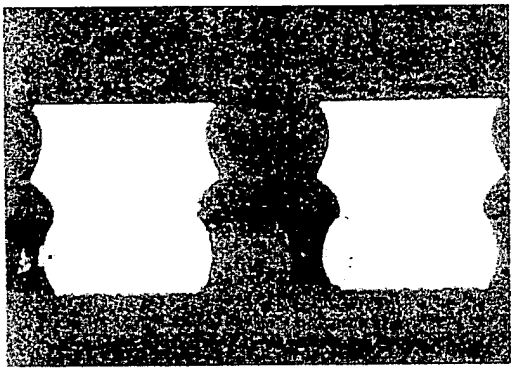

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FIGURE 25. X-section Across Solder Joints

Appendices

APPENDIX 1: BOARD LEVEL RELIABILITY TEST DATA

Temperature Cycle Test

Test Conditions:

- Temperature Range: −40 to 125˚C
- Cycle Duration: 1 hour (15 minute ramp/15 minute Dwell)
- Test Board Dimension: 142.5 mm x 142.5 mm x 1.6 mm
- Test Board Finish: Ni-Au 0.05 µm to 0.127 µm thickness
- Dummy die in package
- Package is bonded with a Daisy Chain Circuit

Failure Determination: Change of 10% in Net Resistance

Results:

24L 4 mm x 5 mm LLP Package
(Package Die Attach Pad soldered to the PCB)

Timepoint	Lot A	Lot B	Lot C
0 Cycles	0/41	0/84	0/83
500 Cycles	0/41	0/84	0/83
1050 Cycles	0/41		

24L 4 mm x 5 mm LLP Package
(Package Die Attach Pad NOT soldered to the PCB)

Timepoint	Lot A	Lot B	Lot C
0 Cycles	0/81	0/78	0/76
500 Cycles	0/81	0/78	0/76
950 Cycles	0/81	0/78	0/76
1050 Cycles	0/81	0/78	0/76

44L 7 mm x 7 mm LLP Package
(Package Die Attach Pad soldered to the PCB)

Timepoint	Lot A	Lot B	Lot C
0 Cycles	0/33	0/69	0/88
500 Cycles	0/33	0/69	0/88
1050 Cycles	0/33	0/69	0/88

44L 7 mm x 7 mm LLP Package
(Package Die Attach Pad NOT soldered to the PCB)

Timepoint	Lot A	Lot B	Lot C
0 Cycles	0/81	0/78	0/76

Appendices (Continued)

Thermal Simulation Conditions (Continued)

Die Size	4.09 x 2.67 x 0.216
DAP Size	4.35 x 3.00
Package Size	6.00 x 5.00 x 1.00
Thermal Vias	0, 2, 4, 8, 12. See *Figure 26.*
Board Size	101.6 x 76.2 x 1.6 (4 layer JEDEC)
Copper Thickness	2.0/1.0/1.0/2.0 oz. (1 oz. = 36 µm)
Copper Coverage	Top layer: traces (27.5 x 0.25) plus metalization area as shown in *Figure 27.* Middle layers: 60.0 x 60.0 Bottom layer: 15% of the board area.

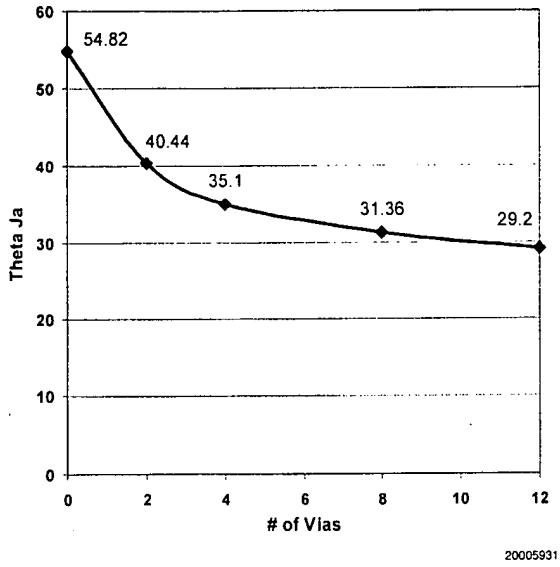

FIGURE 26. θ_{JA} as a Function of Number of Vias Placed in PCB

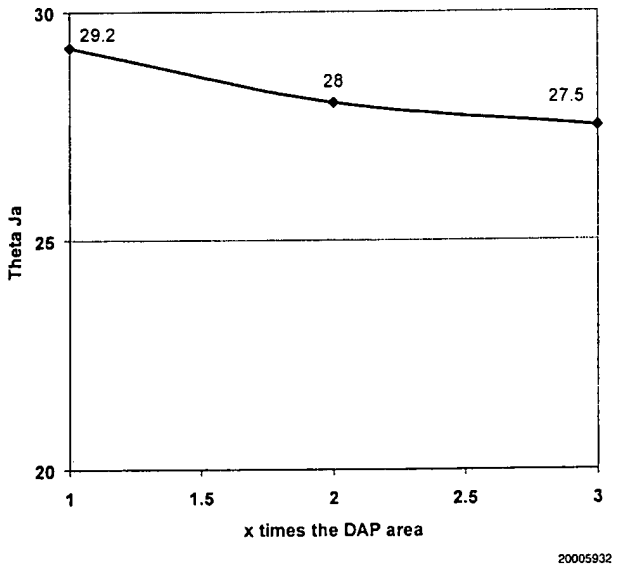

FIGURE 27. θ_{JA} as a Function of Top Metalization Area

Appendices (Continued)

Timepoint	Lot A	Lot B	Lot C
500 Cycles	0/81	0/78	0/76
950 Cycles	0/81	0/78	0/76
1050 Cycles	0/81	0/78	0/76

Standard 56L 9 mm x 9 mm Package
(Power and Ground Ring not soldered to the PCB)

Timepoint	Results
0 Cycles	0/75
500 Cycles	0/75
1050 Cycles	0/75

Lead-Free 56L 9 mm x 9 mm Package
(Power and Ground Ringsoldered to the PCB with SnAgCu solder paste and Sn lead finish)

PCB Finish	750 TMCL	1050 TMCL
NiAu	0/98	0/98
OSP	0/96	0/96

Standard & Lead-Free 56L LLP Board Level TMCL Comparison

Lead Finish	Solder Paste	PCB Finish	750 TMCL	1050 TMCL
Sn	SnPb	NiAu	0/100	0/100
SnPb	SnPb	NiAu	0/100	0/100
Sn	SnPb	OSP	0/99	0/99
SnPb	SnPb	OSP	0/95	0/95
Sn	SnAgCu	NiAu	0/98	0/98
SnPb	SnAgCu	NiAu	0/99	0/99
Sn	SnAgCu	OSP	0/96	0/96

SOT23 5/6L Footprint Compatible LLP

Timepoint	DAP soldered to PCB	DAP not soldered to PCB
0 cycles	0/126	0/84
500 cycles	0/126	0/84
1050 cycles	0/126	0/84

14 Lead Power LLP

Timepoint	Results
0 Cycles	0/80
500 Cycles	0/80
1050 Cycles	0/80

Board Drop Test

Test Conditions:

- Test Board Dimension: 142.5 mm x 142.5 mm x 1.6 mm
- Printed Circuit Board Finish: Ni-Au 2 - 5 micro inches thickness
- Dummy die in package
- Package is bonded with a Daisy Chain Circuit
- Cumulative Dead weight of the board: 150 Grams
- Drop Height: 1.5 meters
- Drop Surface: Non cushioning vinyl tile
- Number of Drops: 30 total
  - — 7 drops: along the length of the PCB
  - — 7 drops: along the width of the PCB
  - — 8 Drops: Along the diagonal of the board
  - — 8 Drops: With the components on the top of the board

Failure Determination: Change of 10% in Net Resistance

Results:

Package Type	Drop Test Results
24L 4 mm x 5 mm LLP (DAP soldered to PCB)	0/20
24L 4 mm x 5 mm LLP (DAP NOT soldered to PCB)	0/20
44L 7 mm x 7 mm LLP (DAP soldered to PCB)	0/20
44L 7 mm x 7 mm LLP (DAP NOT soldered to PCB)	0/20
56L 9 mm x 9 mm LLP (DAP soldered, Power/Ground Rings soldered to PCB)	0/25
14L Power LLP	0/32

Vibration Test

Test Conditions:

- Test Board Dimension: 142.5 mm x 142.5 mm x 1.6 mm
- Printed Circuit Board Finish: Ni-Au 0.05 µm to 0.127 µm thickness
- Dummy die in package
- Package is bonded with a Daisy Chain Circuit
- Die attach pad soldered to PCB
- Vibration test conditions:
  - — Sinusoidal excitation performed for 1 hour at 20G force followed by 3 hours at 40G force
  - — Random Vibration with variable frequencies ranging from 20Hz to 2,000Hz for 3 hours with a force of 2G RMS

Results: DAP Soldered to PCB

Package Type	Test Results
24L 4 mm x 5 mm LLP	0/24
44L 7 mm x 7 mm LLP	0/20
56L 9 mm x 9 mm LLP	0/25
14L 6 mm x 5 mm Power LLP	0/32

APPENDIX 2: THERMAL SIMULATION DATA FOR POWER LLP

Thermal Simulation Conditions

All dimensions are in millimeters